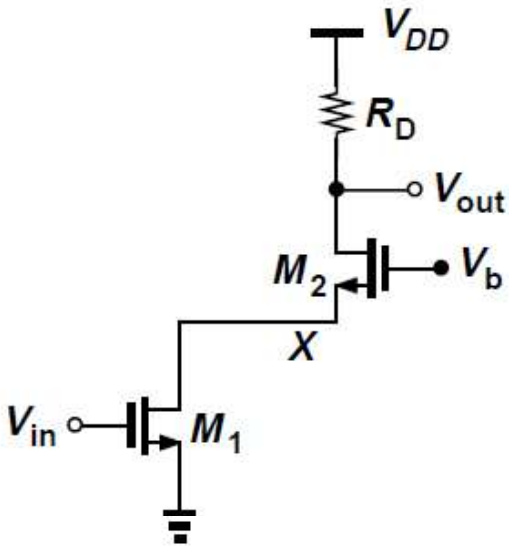
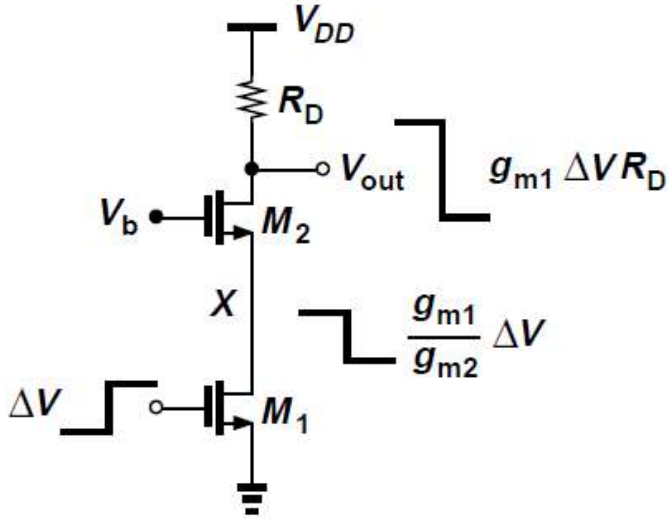
Cascode Stage

- The cascade of a CS stage and a CG stage is called a cascode topology



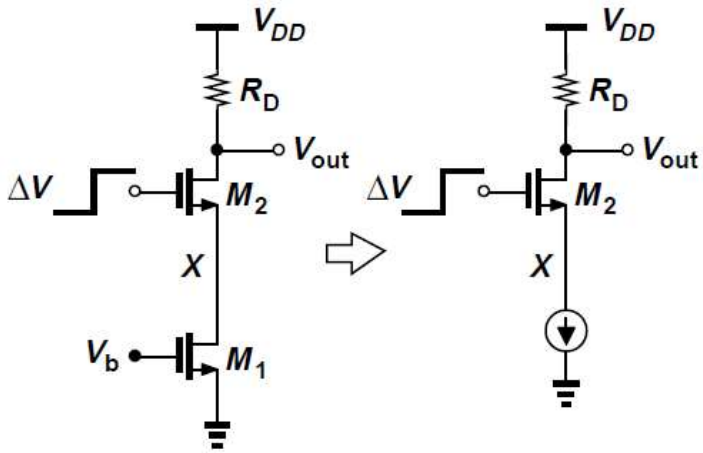
- M_1 generates a small-signal drain current proportional to the small-signal input V_{in} and M_2 simply routes the current to R_D
- M_1 is called the input device and M_2 the cascode device
- M_1 and M_2 in this example carry equal bias and signal currents
  - Topology also called as "telescopic cascode"

Cascode Stage: Qualitative Analysis



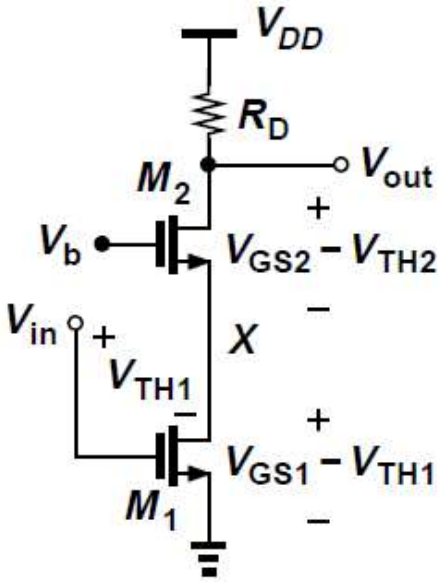
- Assume both transistors are in saturation and $\lambda = \gamma = 0$
- If V_{in} rises by ΔV, then I_{D1} increases by $g_{m1}\Delta V$
- This change in current flows through the impedance seen at X, i.e., the impedance seen at the source of M_2, which is equal to $1/g_{m2}$
- Thus, V_X falls by an amount given by $g_{m1}\Delta V \cdot (1/g_{m2})$
- This change in I_{D1} also flows through R_D, producing a drop of $g_{m1}\Delta V R_D$ in V_{out}, just as in a simple CS stage

Cascode Stage: Qualitative Analysis



- Consider the case when V_{in} is fixed and V_b increases by ΔV
- Since V_{GS1} is constant and $r_{O1}=\infty$, M_1 can be replaced by an ideal current source
- For node X, M_2 operates as a source follower, it senses an input ΔV at its gate and generates an output at X
- With $\lambda = \gamma = 0$, the small-signal voltage of the follower is unity regardless of R_D
- V_X rises by ΔV, *but* V_{out} does not change since $I_{D2}=I_{D1}$=*constant, thus voltage gain from* V_b *to* V_{out} *is zero*

Cascode Stage: Bias Conditions



- For M_1 to operate in saturation, we must have $V_X \geq V_{in} - V_{TH1}$
- If M_1 and M_2 are both in saturation, M_2 operates as a source follower and V_X is primarily determined by V_b: $V_X = V_b - V_{GS2}$
- Thus $V_b - V_{GS2} \geq V_{in} - V_{TH1}$ and hence $V_b > V_{in} + V_{GS2} - V_{TH1}$

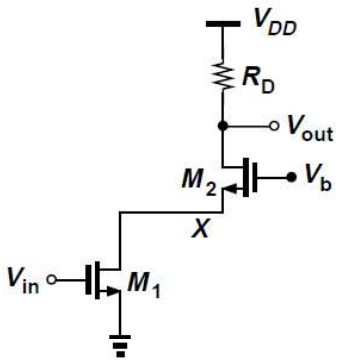
- For M_2 to be saturated, $V_{out} \geq V_b - V_{TH2}$
- Thus,

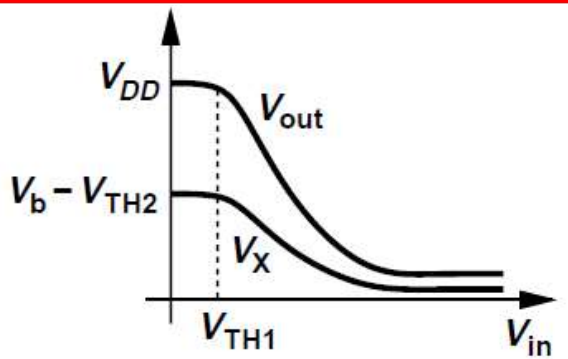
$$\begin{aligned} V_{out} &\geq V_{in} - V_{TH1} + V_{GS2} - V_{TH2} \\ &= (V_{GS1} - V_{TH1}) + (V_{GS2} - V_{TH2}) \end{aligned}$$

if V_b is chosen to place M_1 at the edge of saturation

- Minimum output level for which both transistors are in saturation is equal to the sum of overdrives of M_1 and M_2
- Addition of M_2 to the circuit reduces the output voltage swing by at least its overdrive voltage

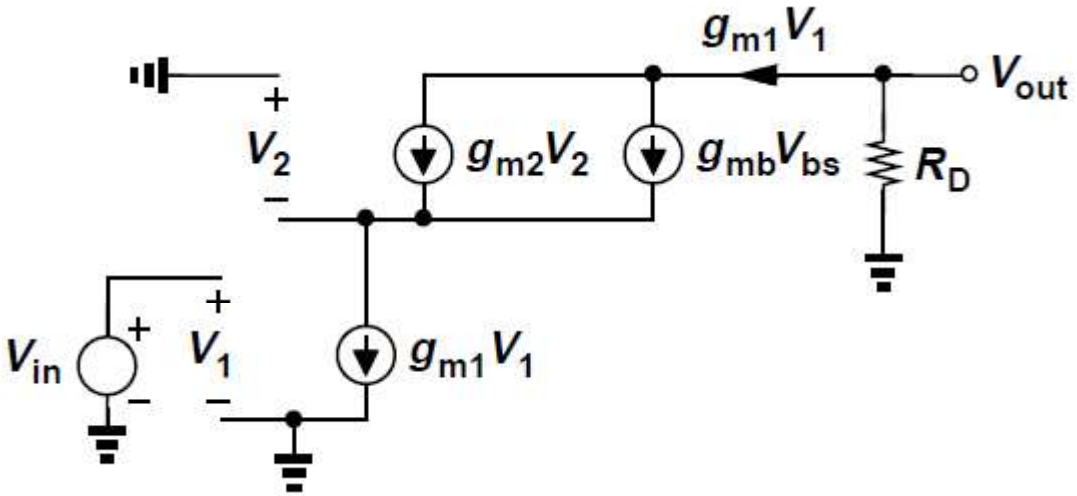
Cascode Stage: Large-Signal Behavior





- For $V_{in} \leq V_{TH1}$, M_1 and M_2 are off, $V_{out}=V_{DD}$, and $V_X \approx V_b - V_{TH2}$
- As V_{in} exceeds V_{TH1}, M_1 draws current, and V_{out} drops
- Since I_{D2} increases, V_{GS2} must increase as well, causing V_X to fall
- As V_{in} becomes sufficiently large, two effects can occur:
  - V_X falls below V_{in} by V_{TH1}, forcing M_1 into the triode region
  - V_{out} drops below V_b by V_{TH2}, driving M_2 into triode region
- Depending on device dimensions and R_D and V_b, one effect may occur before the other

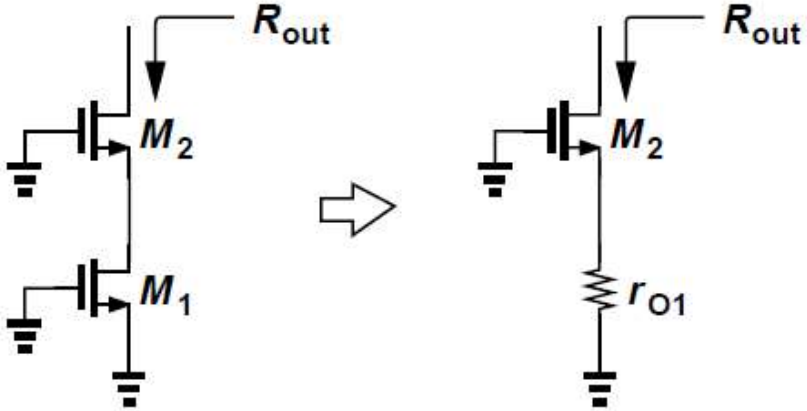
Cascode Stage: Small-signal characteristics



- Assume both transistors operate in saturation and $\lambda=0$
- Voltage gain is equal to that of a common-source stage because the drain current produced by the input device must flow through the cascode device
- This result is independent of the transconductance and body effect of M_2, the cascode device
- Can be verified using $A_v = -G_m R_{out}$

Cascode Stage: Output Impedance

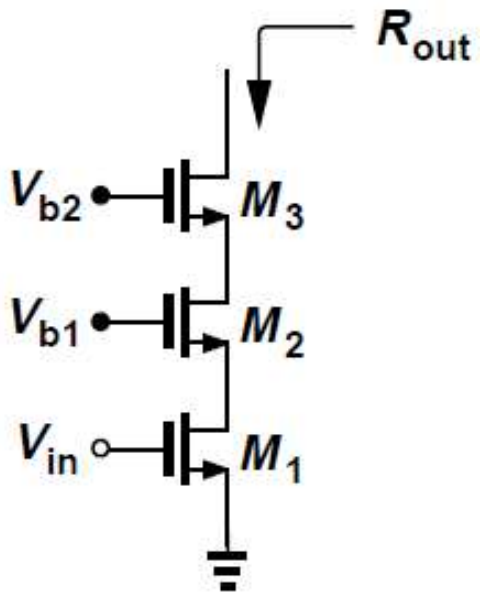
- Important property of the cascode structure is its high output impedance



- For calculation of R_{out}, the circuit can be viewed as a common-source stage with a degeneration resistor equal to r_{O1}
- Thus, $$R_{out} = [1 + (g_{m2} + g_{mb2})r_{O2}]r_{O1} + r_{O2}$$
- Assuming $g_m r_O >> 1$, we have $$R_{out} \approx (g_{m2} + g_{mb2})r_{O2}r_{O1}$$
- M2 boosts the output impedance of M1 by a factor of $(g_{m2}+g_{mb2})r_{O2}$

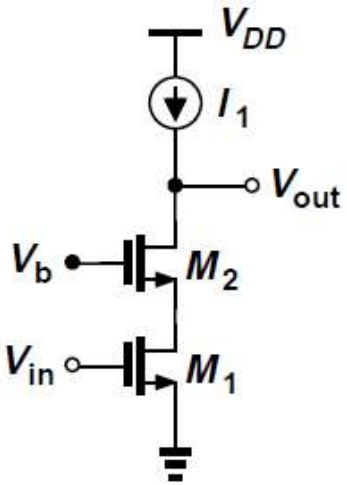
Triple Cascode

- Cascoding can be extended to three or more stacked devices to achieve higher output impedance
- But required additional voltage headroom makes it less attractive
- For a triple cascode, the minimum output voltage is equal to the sum of three overdrive voltages



Cascode stage with current source load

- Voltage gain can be maximized by maximizing G_m and/or R_{out}
- Since G_m is typically determined by the transconductance of a transistor and has trade-offs with the bias current and device capacitances, it is desirable to increase voltage gain by maximizing R

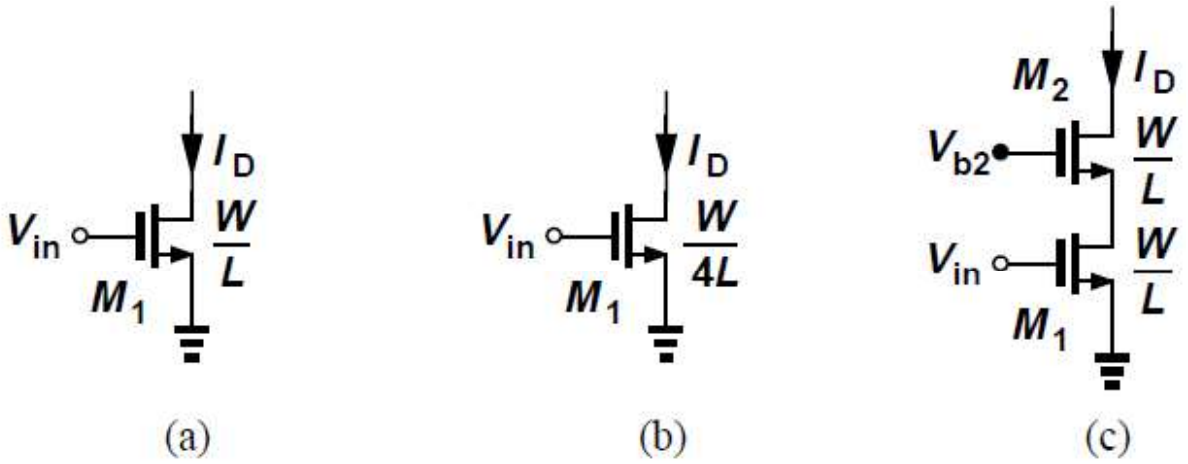


$$G_m \approx g_{m1}$$

$$R_{out} \approx (g_{m2}+g_{mb2})r_{O2}r_{O1}$$

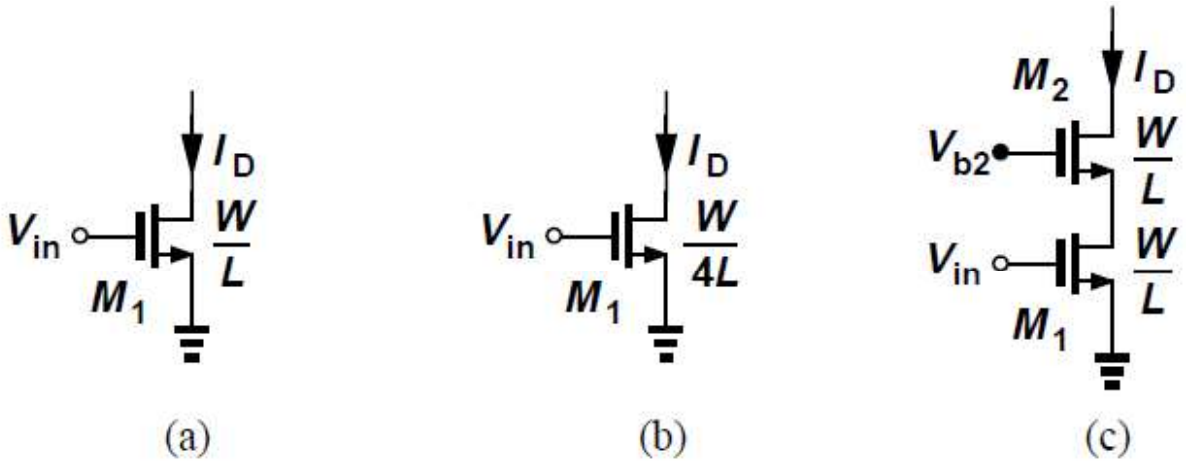
$$A_v = (g_{m2}+g_{mb2})r_{O2}g_{m1}r_{O1}$$

Cascode Stage vs Increasing Length



- **Increasing length of the input transistor for a given bias current increases the output impedance**
- **Suppose the length of the input transistor is quadrupled while the width remains constant**
- **Since $I_D = (1/2)\mu_n C_{ox}(W/L)(V_{GS} - V_{TH})^2$, the overdrive voltage is doubled and the transistor consumes the same amount of voltage headroom as does a cascode stage, i.e., circuits in (b) and (c) impose equal voltage swing constraints**

Cascode Stage vs Increasing Length

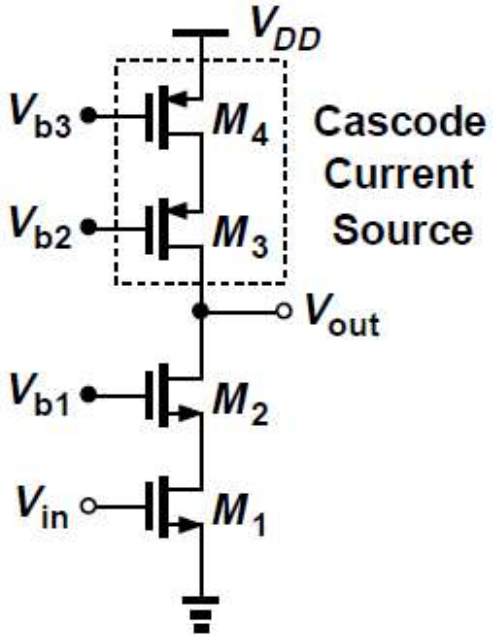


- **Since**

$$g_m r_O = \sqrt{2\mu_n C_{ox} \frac{W}{L} I_D} \frac{1}{\lambda I_D}$$

- **And $\lambda \propto 1/L$, quadrupling *L* only doubles the value of $g_m r_O$ while cascoding results in an output impedance of roughly $g_m r_O^2$**
- **Transconductance of M_1 in (b) is only half of that in (c), degrading the performance**
- **For a given voltage headroom, the cascode structure provides a higher output impedance**

Cascode Structure as Current Source



- High output impedance of cascode structure yields a current source closer to the ideal, but at the cost of voltage headroom
- The current source load in a cascode stage can be implemented as a PMOS cascode, exhibiting an impedance equal to

$$[1 + (g_{m3} + g_{mb3})r_{O3}]r_{O4} + r_{O3}$$

- To find the voltage gain, $G_m \approx g_{m1}$
- Rout is the parallel combination of the NMOS and PMOS cascode output impedances

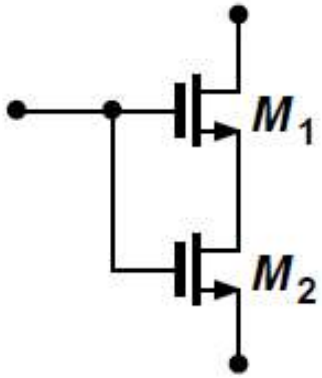
$$R_{out} = \{[1 + (g_{m2} + g_{mb2})r_{O2}]r_{O1} + r_{O2}\} \| \{[1 + (g_{m3} + g_{mb3})r_{O3}]r_{O4} + r_{O3}\}$$

- The gain is given by $|A_v| \approx g_{m1}R_{out}$
- For typical values, this is approximated as

$$|A_v| \approx g_{m1}[(g_{m2}r_{O2}r_{O1}) \| (g_{m3}r_{O3}r_{O4})]$$

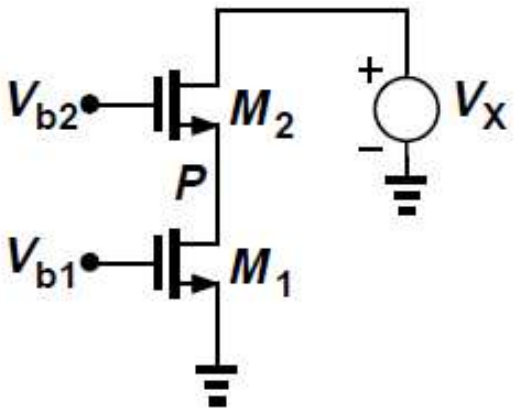
Poor Man's Cascode

- A "minimalist" cascode current source omits the bias voltage necessary for the cascode device



- Called "poor man's cascode", M_2 is placed in the triode region because $V_{GS1}>V_{TH1}$ and $V_{DS2}=V_{GS2}-V_{GS1} < V_{GS2}-V_{TH2}$
- If M_1 and M_2 have the same dimensions, the structure is equivalent to a single transistor having twice the length-not really a cascode
- In modern CMOS technologies, transistors with different threshold voltages are allowable, allowing M_2 to operate in saturation if M_1 has a lower threshold than M_2

Poor Man's Cascode: Shielding Property



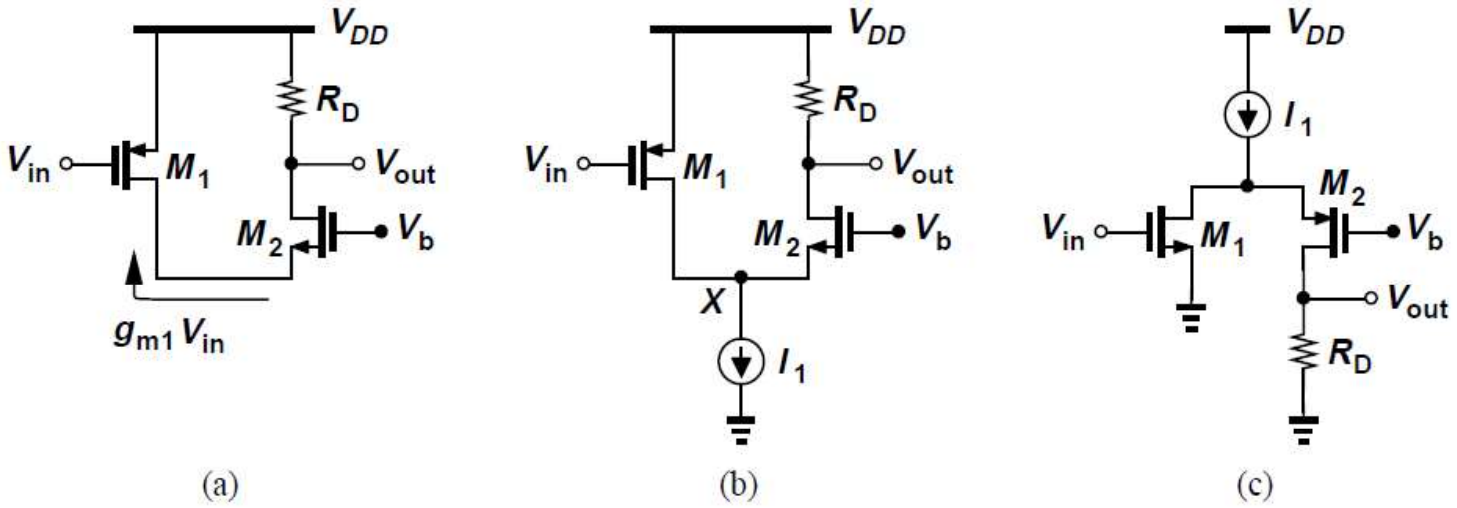
- High output impedance arises from the fact that if the output node voltage is changed by ΔV, the resulting change at the source of the cascode device is much less
  - Cascode transistor "shields" the input device from voltage variations at the output
- Shielding property diminishes if cascode device enters triode region
- In above circuit, as V_X falls below V_{b2}-V_{TH2}, M_2 enters triode region and requires a greater gate-source overdrive to sustain the current drawn by M_1 therefore

$$I_{D2} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_2 [2(V_{b2} - V_P - V_{TH2})(V_X - V_P) - (V_X - V_P)^2]$$

- As V_X decreases, V_P also drops to keep I_{D2} constant so variation of V_X is less attenuated as it appears at P

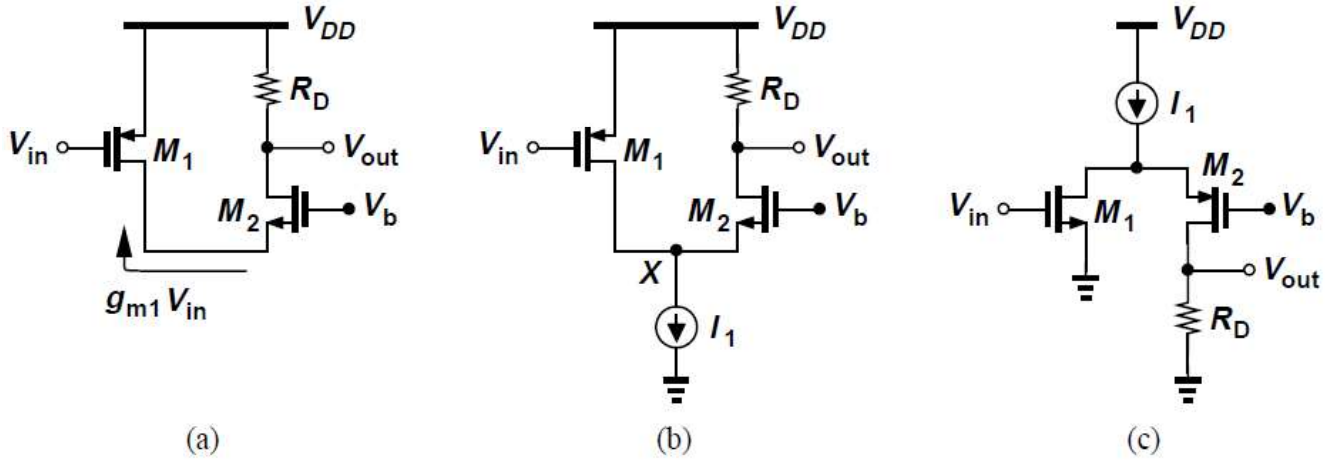
Folded Cascode

- The input device and the cascode device in a cascode structure need not be of the same type



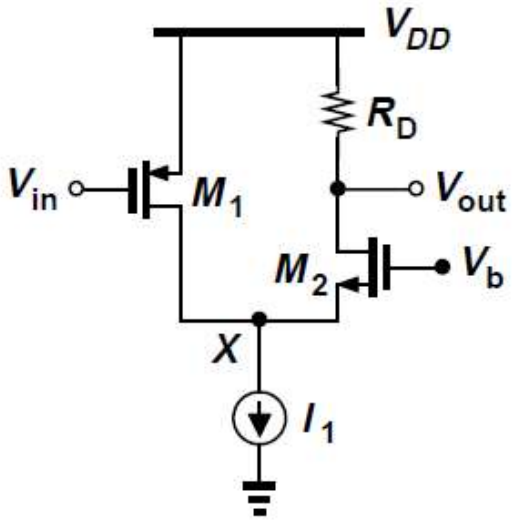
- In the figure above, (a) shows a PMOS-NMOS cascode combination that performs the same function as a telescopic cascode
- In order to bias M_1 and M_2, a current source must be added as shown in (b)
- $|I_{D1}| + I_{D2}$ is equal to I_1 and hence constant
- (c) shows an NMOS-PMOS folded cascode

Folded Cascode: Small-signal operation



- If V_{in} becomes more positive, $|I_{D1}|$ decreases, forcing I_{D2} to increase and hence V_{out} to drop
- The voltage gain and output impedance can be obtained as calculated for the NMOS-NMOS cascode shown earlier
- (b) and (c) are called "folded cascode" stages because the small-signal current is "folded" up [in (b)] or down [in (c)]
- In the telescopic cascode, the bias current is reused whereas those of M_1 and M_2 add up to I_1 in (b) and (c), leading to a higher bias current

Folded Cascode: Large-signal operation

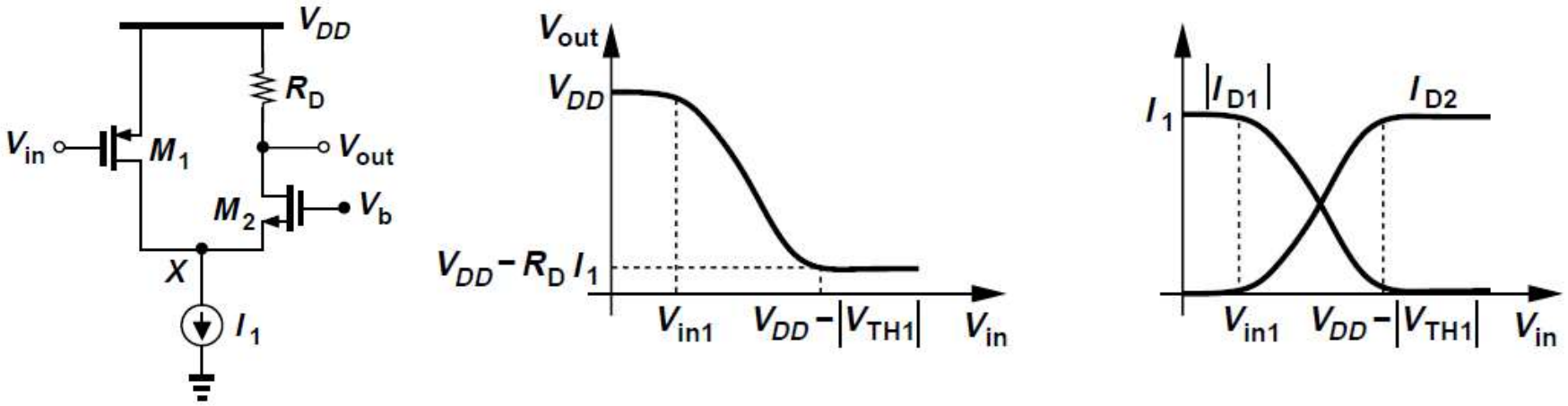


- Suppose V_{in} decreases from V_{DD} to zero
- For $V_{in} > V_{DD}-|V_{TH1}|$, M_1 is off and M_2 carries all of I_1, yielding $V_{out} = V_{DD} - I_1R_D$
- For $V_{in} < V_{DD} - |V_{TH1}|$, M_1 turns on in saturation, giving

$$I_{D2} = I_1 - \frac{1}{2}\mu_p C_{ox}\left(\frac{W}{L}\right)_1 (V_{DD} - V_{in} - |V_{TH1}|)^2.$$

- As V_{in} drops, I_{D2} decreases further, falling to zero if $I_{D1}=I_1$

Folded Cascode: Large-signal operation



- This occurs at $V_{in} = V_{in1}$ if

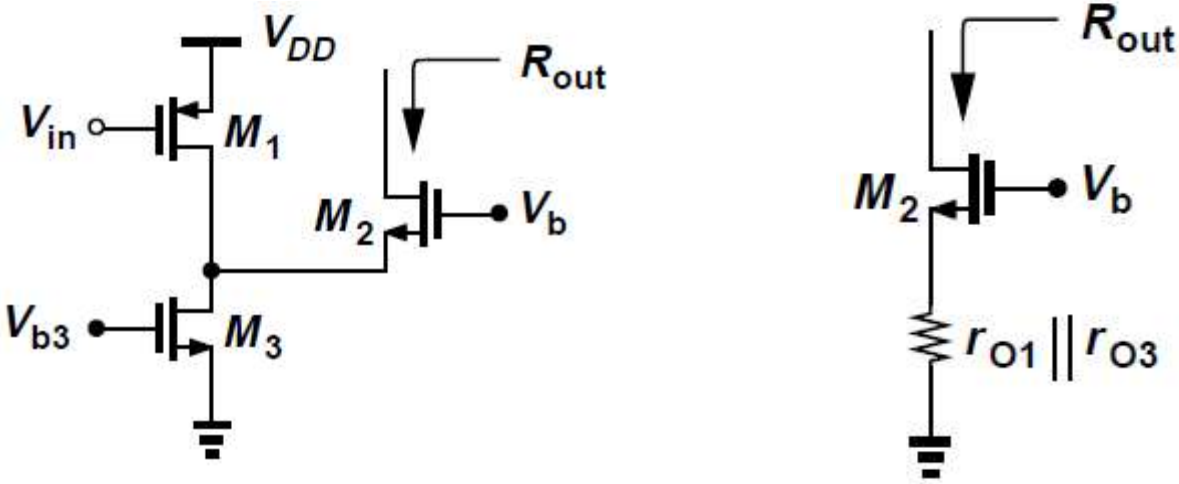
$$\frac{1}{2}\mu_p C_{ox}\left(\frac{W}{L}\right)_1 (V_{DD} - V_{in1} - |V_{TH1}|)^2 = I_1$$

- Thus,

$$V_{in1} = V_{DD} - \sqrt{\frac{2I_1}{\mu_p C_{ox}(W/L)_1}} - |V_{TH1}|$$

- If V_{in} falls below this level, I_{D1} tends to be greater than I_1 and M_1 enters the triode region to ensure $I_{D1}=I_1$
- As I_{D2} drops, V_X rises, reaching V_b-V_{TH2} for $I_{D2}=0$
- As M_1 enters the triode region, V_X approaches V_{DD}

Folded Cascode: Output Impedance



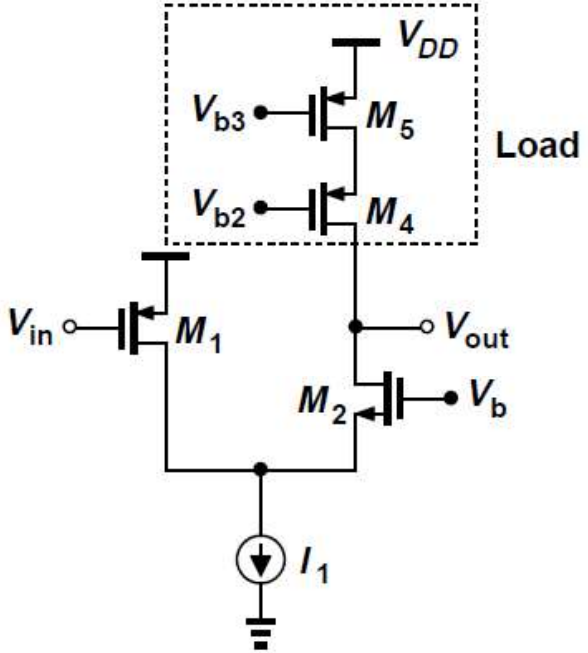
- M_3 operates as the bias current source
- Using earlier results,

$$R_{out} = [1 + (g_{m2} + g_{mb2})r_{O2}](r_{O1} \| r_{O3}) + r_{O2}$$

- The circuit exhibits a lower output impedance than a nonfolded (telescopic) cascode

Folded Cascode with cascode load

- To achieve a high voltage gain, the load of a folded cascode can be implemented as a cascode itself



- Increasing the output resistance of voltage amplifiers to obtain a high gain may make the speed of the circuit susceptible to the load capacitance
- A high output impedance itself does not pose a serious issue if the amplifier is placed in a proper feedback loop