Short Channel Effects

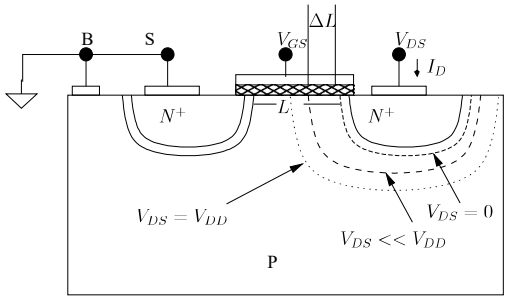


Figure: NMOS Transistor with Short Channel Effects

- Drain is very close to the source (L is very small)
- The depletion regions in the drain and source are comparable to the channel length

Channel Length Modulation

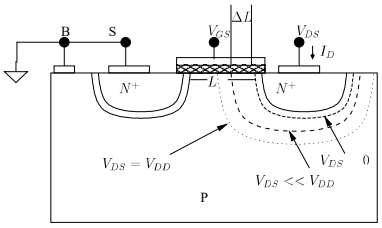


Figure: NMOS Transistor with Short Channel Effects

$$I_D = \frac{k_n^{'}}{2}\frac{W}{L-\Delta L}[(V_{GS}-V_{TH})^2]$$

$$I_D = \frac{k_n^{'}}{2}\frac{W}{L}[(V_{GS}-V_{TH})^2](1+\frac{\Delta L}{L})$$

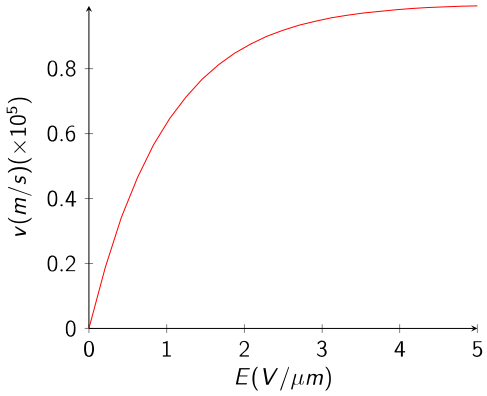
$$I_D = \frac{k_n^{'}}{2}\frac{W}{L}[(V_{GS}-V_{TH})^2](1+\lambda V_{DS})$$

Velocity Saturation

$$v_n = \mu_n E_{Lat}$$

- Not entirely correct - Velocity does not linearly increase with lateral field for ever
- It saturates beyond a critical field E_{Crit}
- Electrons encounter more collisions and hence don't pick up speed
- Maximum velocity of electrons/ holes $= 10^5 m/s$

Velocity Saturation



$$v = \begin{cases} \frac{\mu E}{1+\frac{E}{E_C}} & \text{if } E \leq E_C \\ v_{sat} & \text{if } E > E_C \end{cases}$$

Velocity Saturation- Simplified

Velocity:

$$v = \begin{cases} \mu E & \text{if } E \leq E_C \\ v_{sat} = \mu E_C & \text{if } E > E_C \end{cases}$$

VDS Saturation :

$$V_{DS-SAT} = L * E_C = \frac{L v_{SAT}}{\mu}$$

Velocity Saturated Drain Current:

$$I_{DS-SAT} = I_{DS}(V_{DS} = V_{DS-SAT})$$

$$I_{DS-SAT} = \mu_n C_{OX} \frac{W}{L} \left((V_{GS} - V_{TH}) V_{DS-SAT} - \frac{V_{DS-SAT}^2}{2} \right)$$

Unified Current Model

- Useful to combine all effects into one equation
- Voltage values determine the governing equations

$$I_{DS} = \begin{cases} 0 & |V_{GS}| < |V_{TH}| \\ k' \frac{W}{L} \left((V_{GS} - V_{TH}) V_{min} - \frac{V_{min}^2}{2} \right) (1 + \lambda V_{DS}) & |V_{GS}| > |V_{TH}| \end{cases}$$

Where

$$V_{min} = min(V_{DS}, (V_{GS} - V_{TH}), V_{DS-SAT}) \ldots NMOS$$
$$V_{min} = max(V_{DS}, (V_{GS} - V_{TH}), V_{DS-SAT}) \ldots PMOS$$
$$V_{TH} = V_{TH0} + \gamma(\sqrt{|V_{SB} + \Psi_S|} - \sqrt{\Psi_S})$$

$(V_{TH0}, k', V_{DSAT}, \gamma, \lambda)$ - Technology parameters

Sub-threshold Leakage

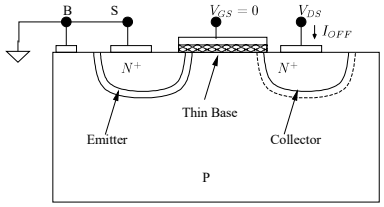
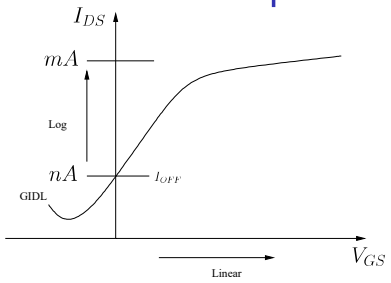


Figure: NMOS Transistor Sub-Threshold Leakage

- In a short channel transistor, the thin channel acts like a thin base of a BJT.
- Diffusion current flows even when $V_{GS} = 0$.
- Exponential dependence on V_{GS}

$$I_{OFF} = I_S e^{\frac{V_{GS}-V_{TH}}{nkT/q}} \left(1 - e^{-\frac{V_{DS}}{kT/q}}\right)(1 + \lambda V_{DS})$$

Sub-threshold Slope



$$S = \frac{1}{\frac{d(log_{10}(I_{OFF}))}{dV_{GS}}}$$

$$S = n\frac{kT}{q}ln(10)$$

- Ideal transistor $n = 1$, $S_{min} = 60mV/decade$
- Actual transistors $n \approx 1.5$ and hence $S = 90mV/decade$

Gate Induced Drain Leakage (GIDL)

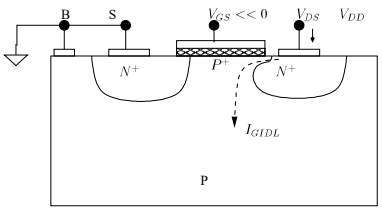


Figure: NMOS Transistor with Halo Implant

- Negative V_{GS} exponentially reduces sub-threshold leakage
- But beyond a point GIDL kicks in
- Surface is in deep accumulation causing a deeper depletion in the diffusion
- Tunneling current from drain to substrate

Drain Induced Barrier Lowering (DIBL)

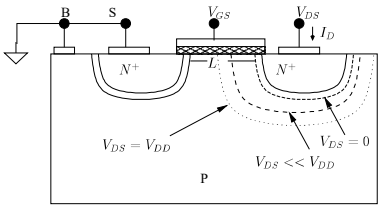


Figure: NMOS Transistor DIBL

- Drain controls amount of depletion in the channel
- Easier for the gate to invert with higher V_{DS}
- Gate effectively has lesser control

Drain Induced Barrier Lowering (DIBL)

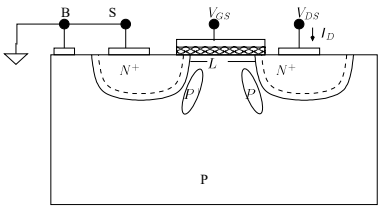


Figure: NMOS Transistor with Halo Implant

- P^+ halo added near diffusion
- Depletion layer now goes deeper into the diffusion rather than channel
- Gate has better control now
- $DIBL = \frac{V_{TH}(V_{DS}=V_{DD}^H)-V_{TH}(V_{DS}=V_{DD}^L)}{V_{DD}^H-V_{DD}^L}$