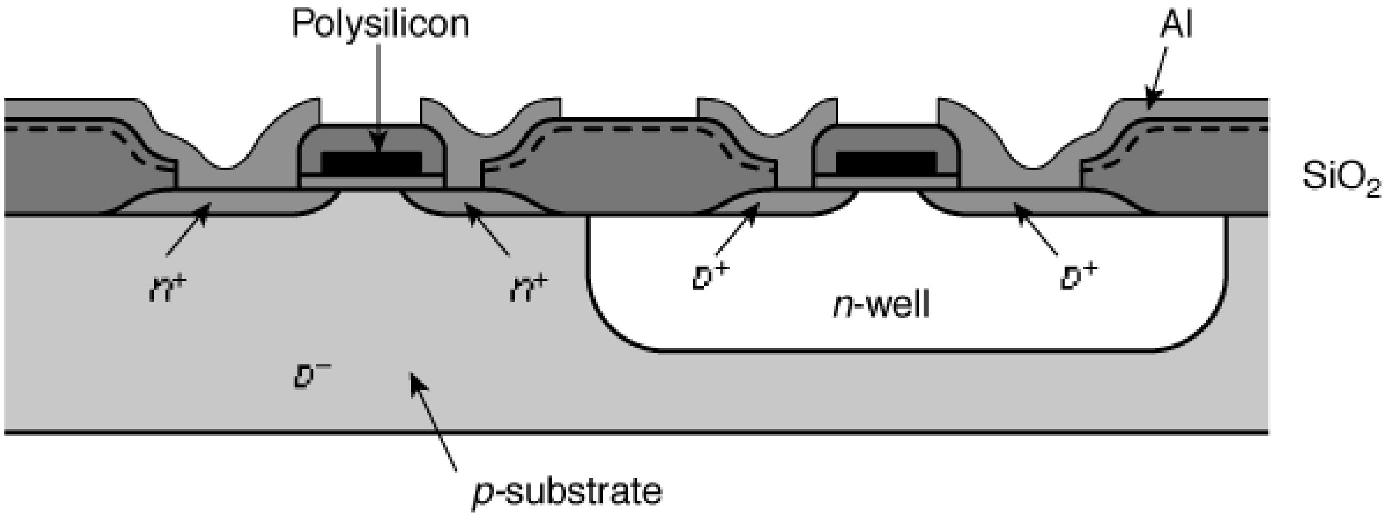
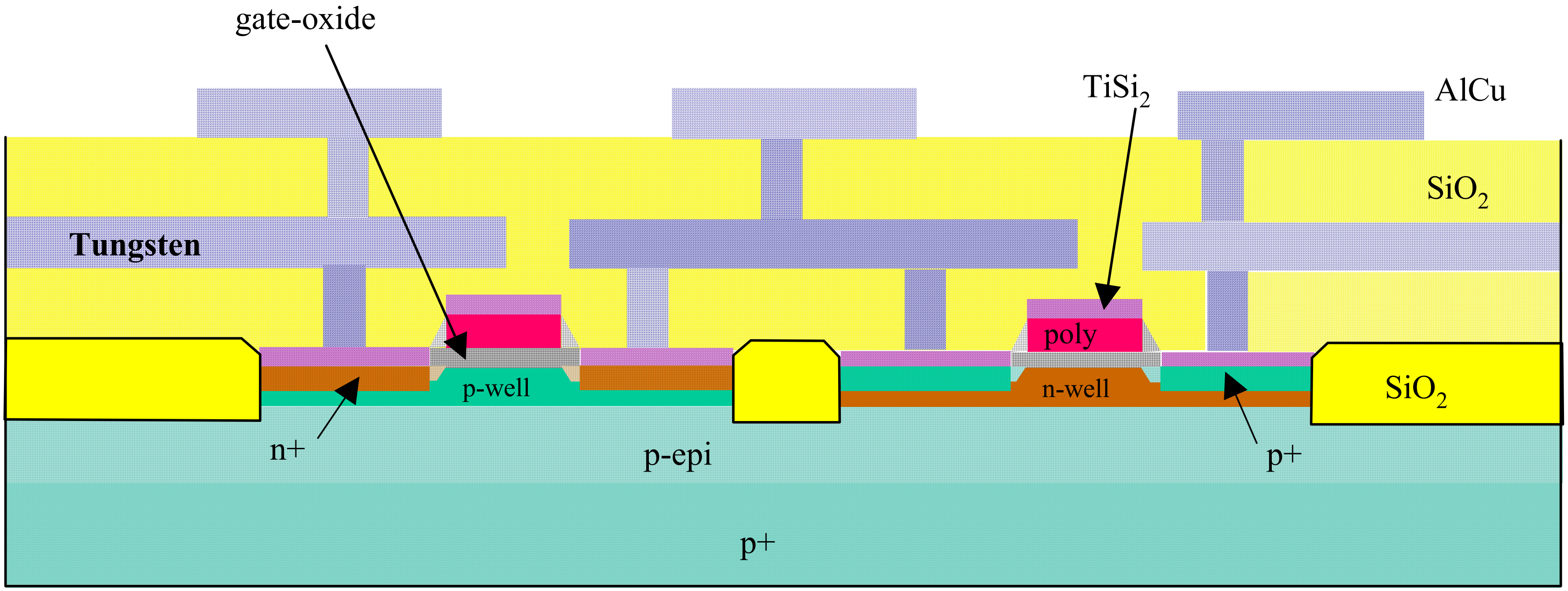
CMOS Process

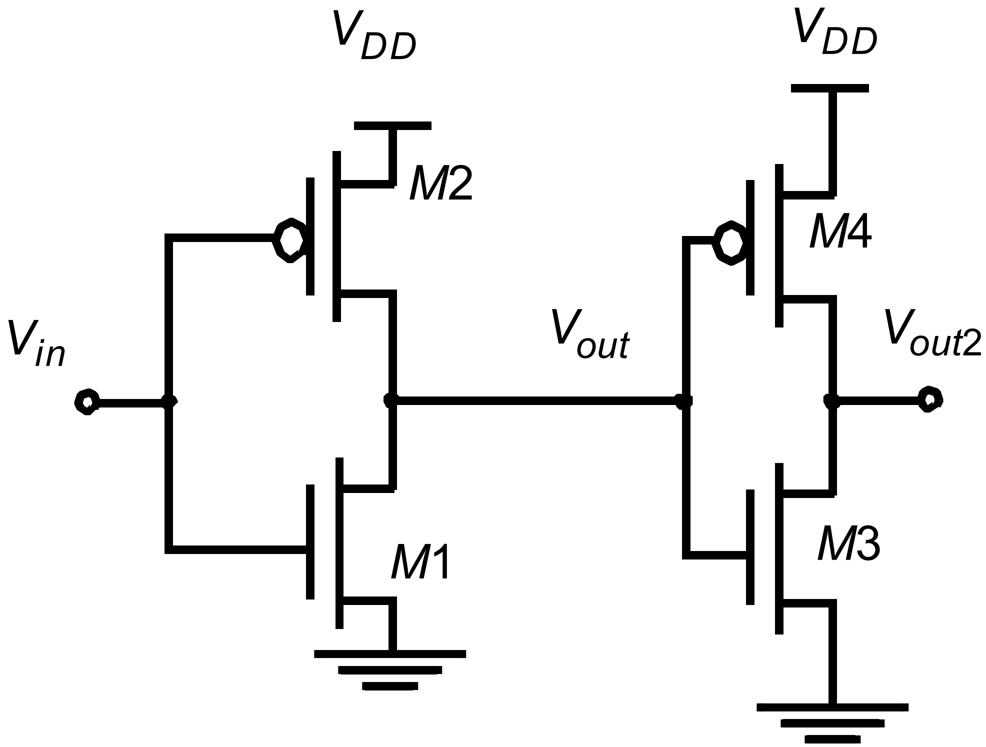


A Modern CMOS Process

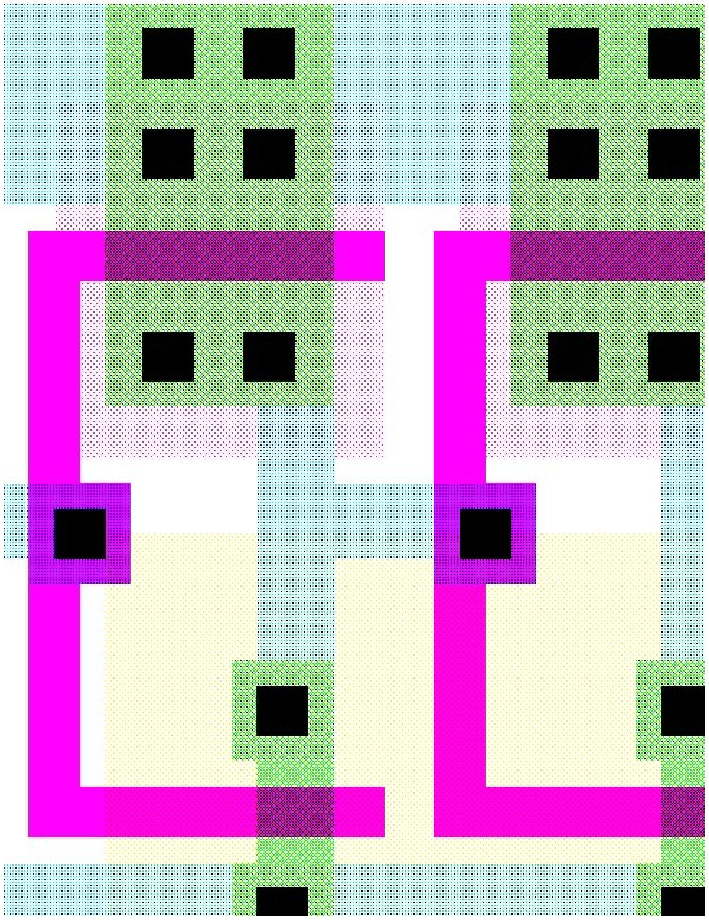


Dual-Well Trench-Isolated CMOS Process

Circuit Under Design



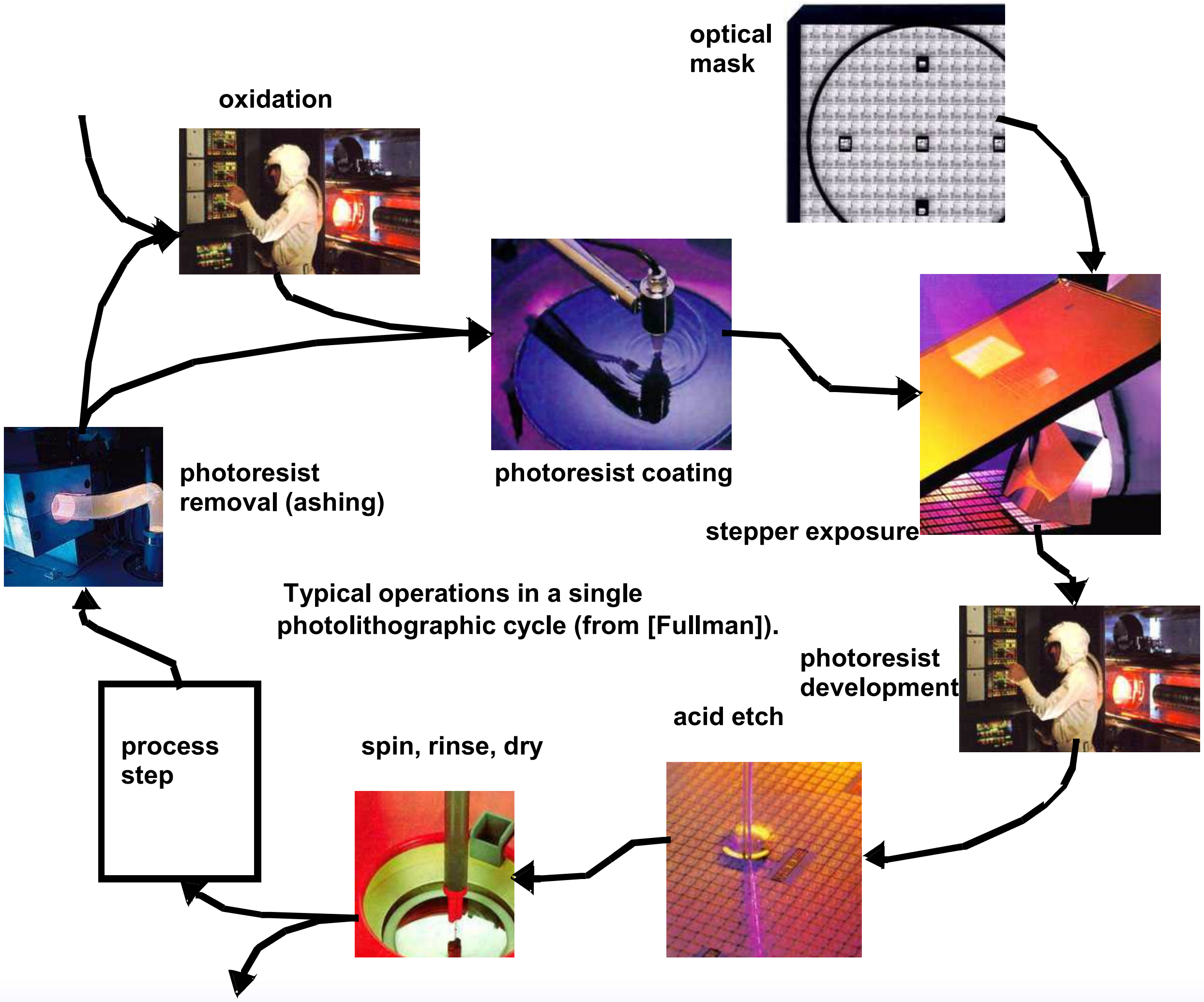
Its Layout View



The Manufacturing Process

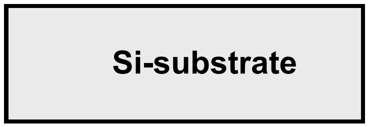
For a great tour through the IC manufacturing process and its different steps, check http://www.fullman.com/semiconductors/semiconductors.html

Photo-Lithographic Process

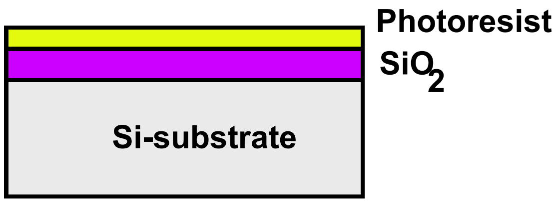


Typical operations in a single photolithographic cycle (from [Fullman]).

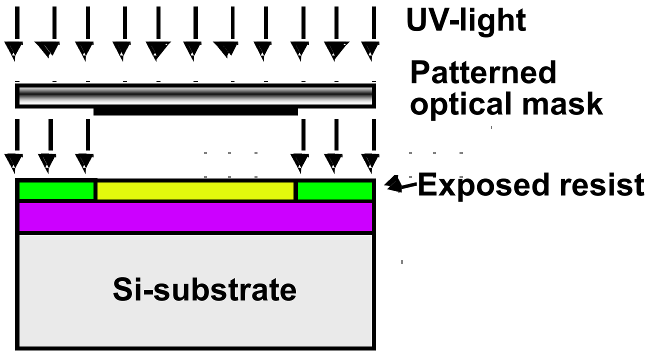
Patterning of SiO2



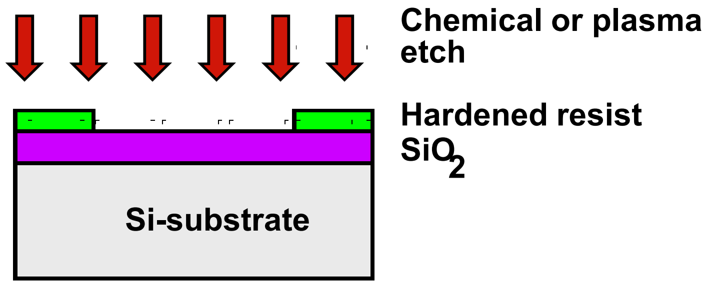
(a) Silicon base material



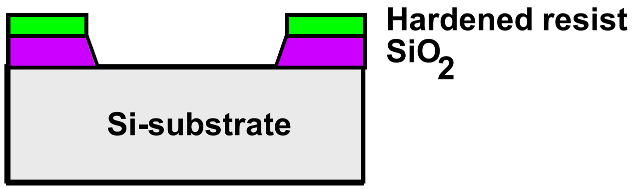
(b) After oxidation and deposition of negative photoresist



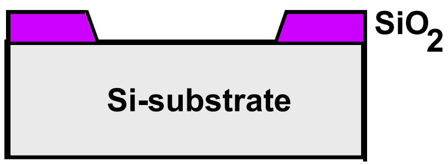
(c) Stepper exposure



(d) After development and etching of resist, chemical or plasma etch of SiO_2



(e) After etching



(f) Final result after removal of resist

CMOS Process at a Glance

Define active areas
Etch and fill trenches

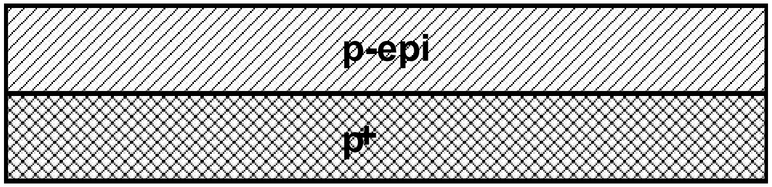
Implant well regions

Deposit and pattern polysilicon layer

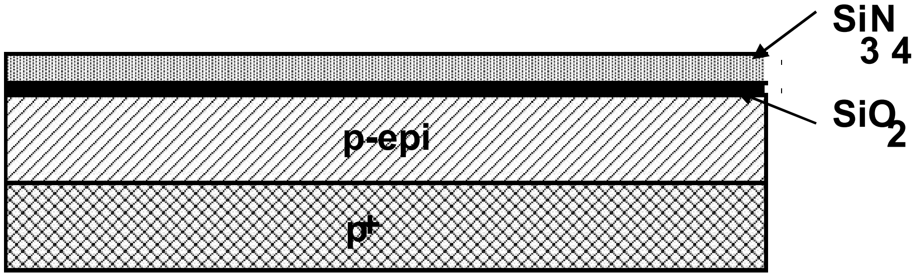
Implant source and drain regions and substrate contacts

Create contact and via windows
Deposit and pattern metal layers

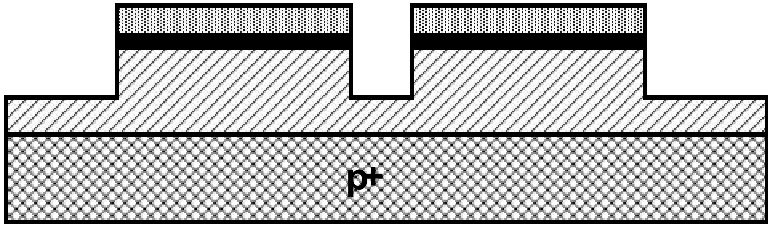
CMOS Process Walk-Through



(a) Base material: p+ substrate with p-epi layer

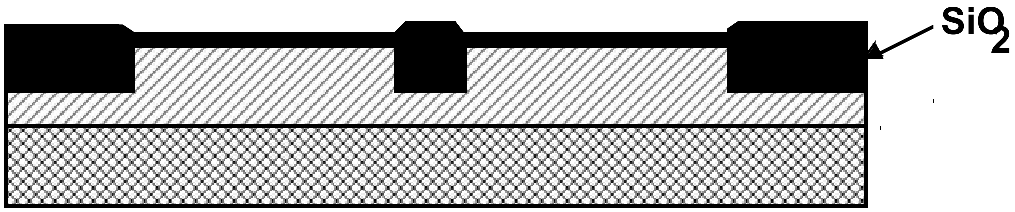


(b) After deposition of gate-oxide and sacrificial nitride (acts as a buffer layer)

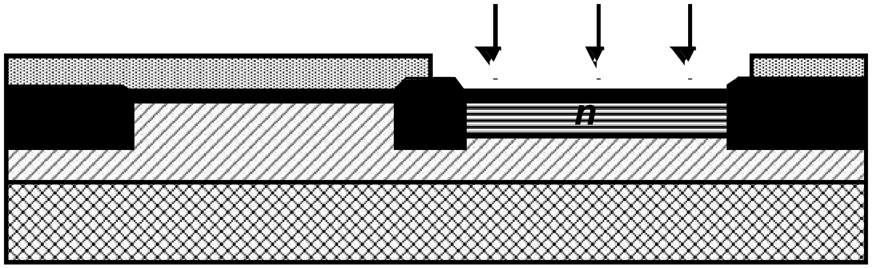


(c) After plasma etch of insulating trenches using the inverse of the active area mask

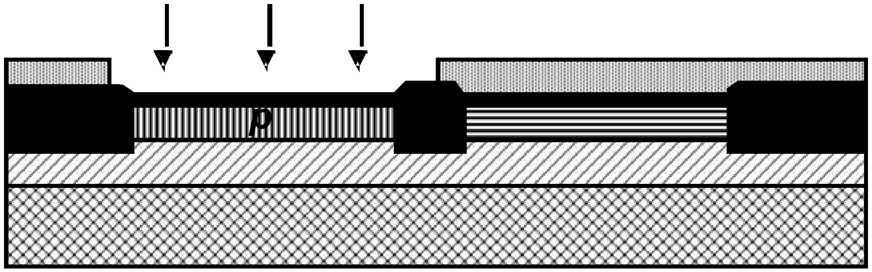
CMOS Process Walk-Through



(d) After trench filling, CMP planarization, and removal of sacrificial nitride

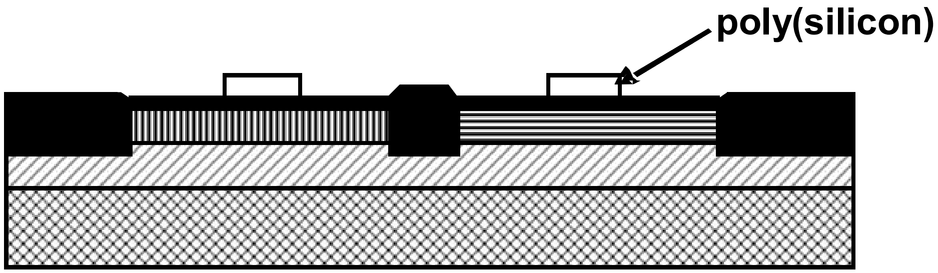


(e) After n-well and V_{Tp} adjust implants

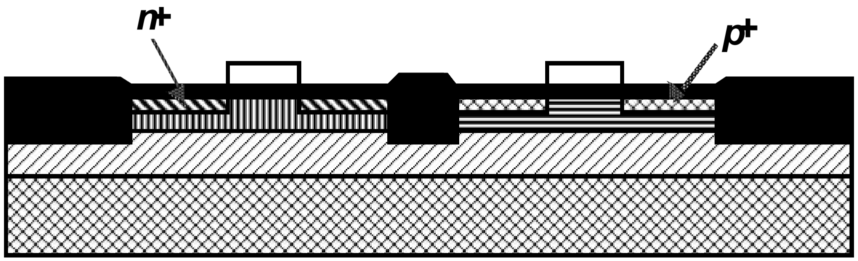


(f) After p-well and V_{Tn} adjust implants

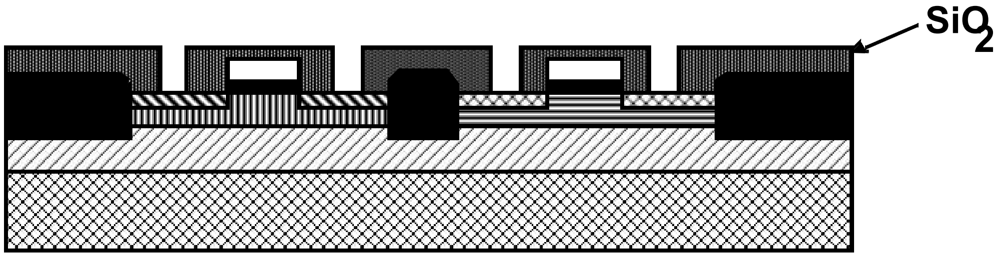
CMOS Process Walk-Through



(g) After polysilicon deposition and etch

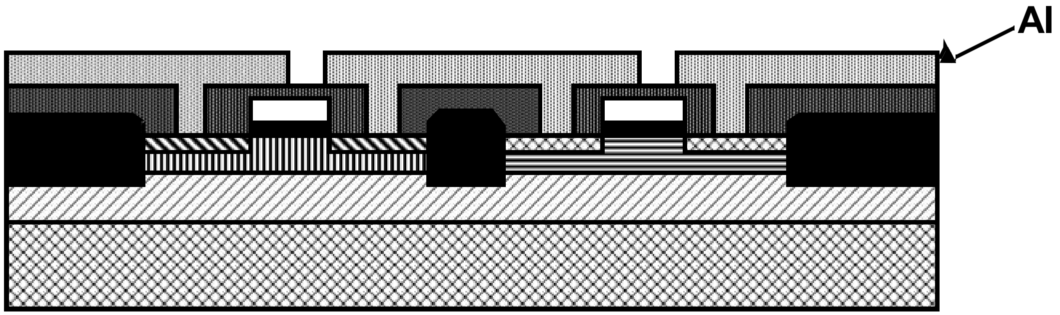


(h) After *n*+ source/drain and *p*+ source/drain implants. These steps also dope the polysilicon.

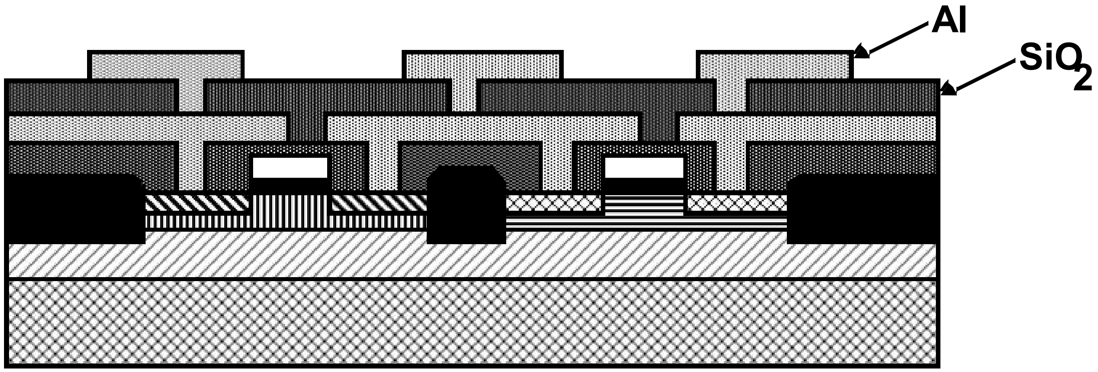


(i) After deposition of SiO$_2$ insulator and contact hole etch.

CMOS Process Walk-Through

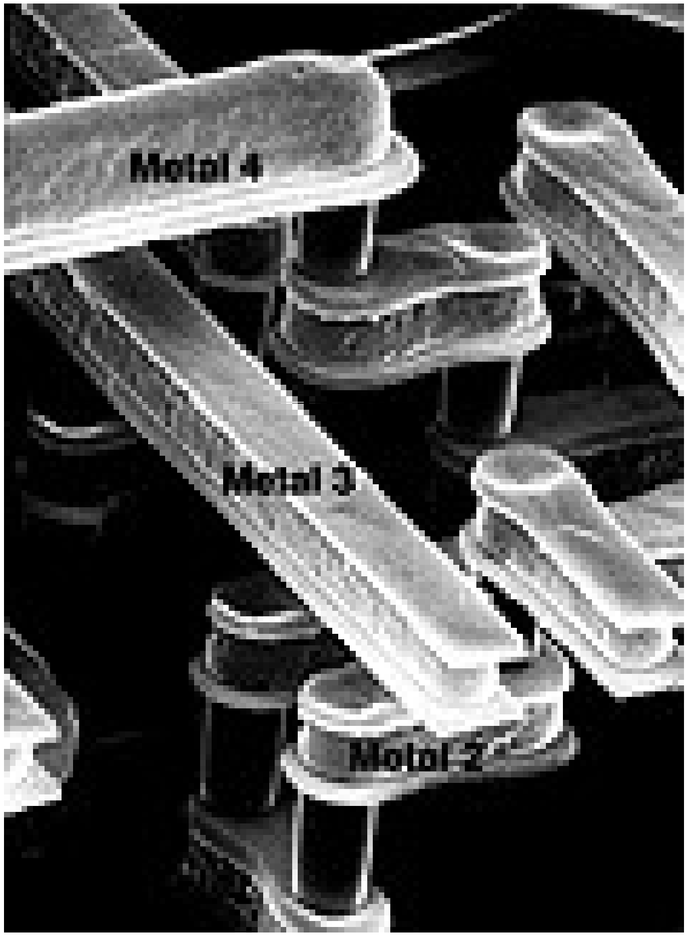


(j) After deposition and patterning of first Al layer.

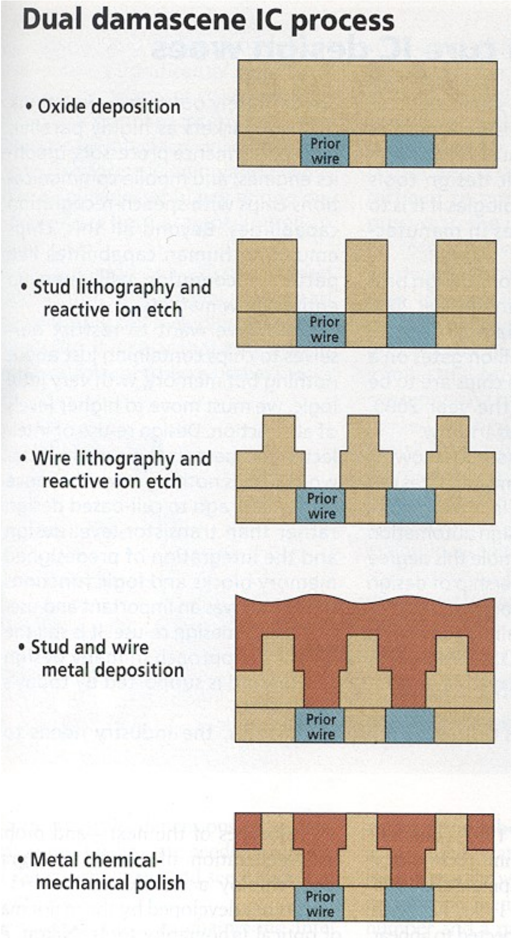


(k) After deposition of SiO_2 insulator, etching of via's, deposition and patterning of second layer of Al.

Advanced Metallization



Advanced Metallization



Source: IBM Corp.