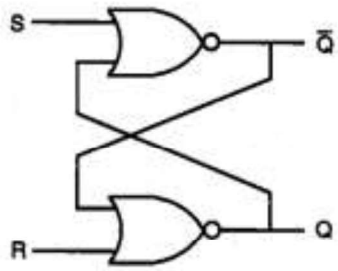
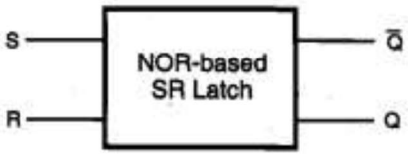
SR Latch Circuit

- the circuit structure of the simple CMOS SR latch, which has two such triggering inputs, S (set) and R (reset).
- the SR latch is also called an SR flip-flop, since two stable states can be switched back and forth.
- The circuit consists of two CMOS NOR2 gates.
- One of the input terminals of each NOR gate is used to cross-couple to the output of the other NOR gate, while the second input enables triggering of the circuit.





Truth table of NOR based SR latch circuit

S	R	Q_{n+1}	$\overline{Q}_{n+1}$	Operation
0	0	Q_n	$\overline{Q_n}$	Hold
1	0	1	0	Set
0	1	0	1	Reset
1	1	0	0	Not allowed

if S is equal to "0" and R is equal to " 1," then the output node Q will be forced to "0" while Q is forced to "1.“

Thus, with this input combination, the latch is reset, regardless of its previously held state.

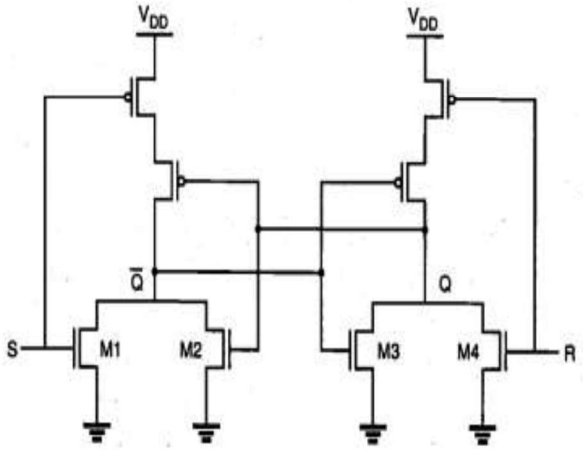
Finally, consider the case in which both of the inputs S and R are equal to logic “1 .“

In this case, both output nodes will be forced to logic "0," which conflicts with the complementarity of Q and Q.

Therefore, this input combination is not permitted during normal operation and is considered to be a not allowed condition.

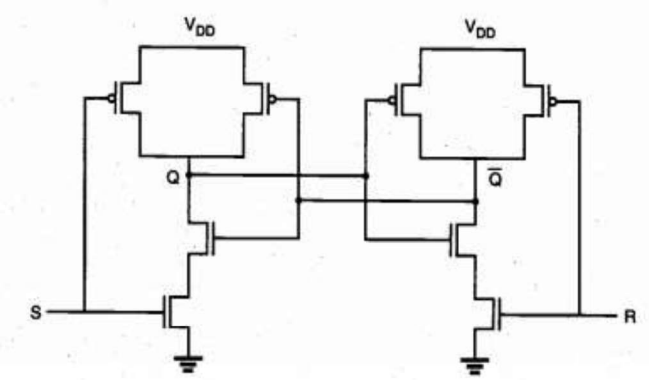
Operation of the CMOS SR Latch

- If the set input (S) is equal to VOH and the reset input (R) is equal to VOL, both of the parallel-connected transistors Ml and M2 will be on. Consequently, the voltage on node Q will assume a logic-low level of VOL = 0.
- At the same time, both M3 and M4 are turned off, which results in a logic-high voltage VOH at node Q. If the reset input (R) is equal to VOH and the set input (S) is equal to VOL, the situation will be reversed (Ml and M2 turned off and M3 and M4 turned on).
- When both of the input voltages are equal to VOL' on the other hand, there are two possibilities. Depending on the previous state of the SR latch, either M2 or M3 will be on, while both of the trigger transistors MI and M4 are off. This will generate a logic-low level of VOL = O at one of the output nodes, while the complementary output node is at VOH.

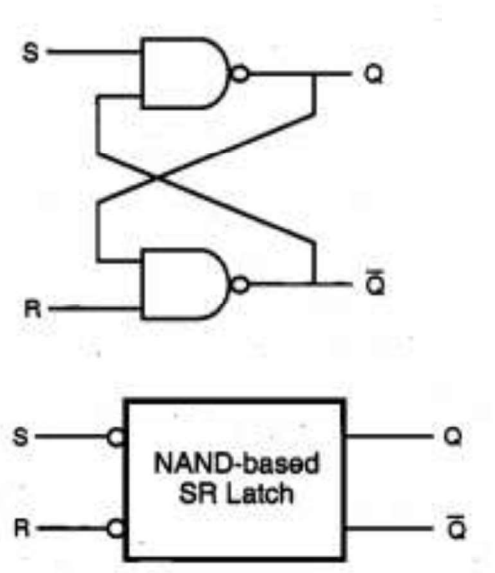


S	R	Q_{n+1}	$\overline{Q_{n+1}}$	Operation
V_{OH}	V_{OL}	V_{OH}	V_{OL}	M1 and M2 on, M3 and M4 off
V_{OL}	V_{OH}	V_{OL}	V_{OH}	M1 and M2 off, M3 and M4 on
V_{OL}	V_{OL}	V_{OH}	V_{OL}	*M*1 and M4 off, M2 on, or
V_{OL}	V_{OL}	V_{OL}	V_{OH}	M1 and M4 off, M3 on

SR Latch with NAND gate

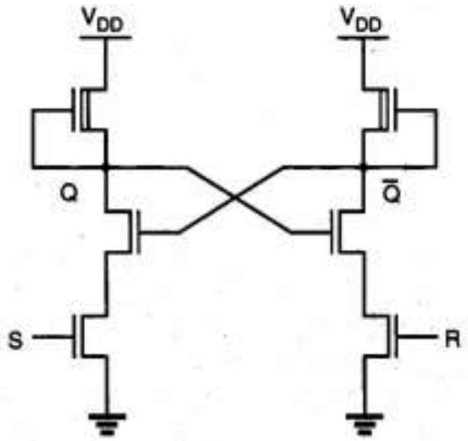


S	R	Q_{n+1}	$\overline{Q_{n+1}}$	Operation
0	0	1	1	not allowed
0	1	1	0	set
1	0	0	1	reset
1	1	Q_n	$\overline{Q_n}$	hold

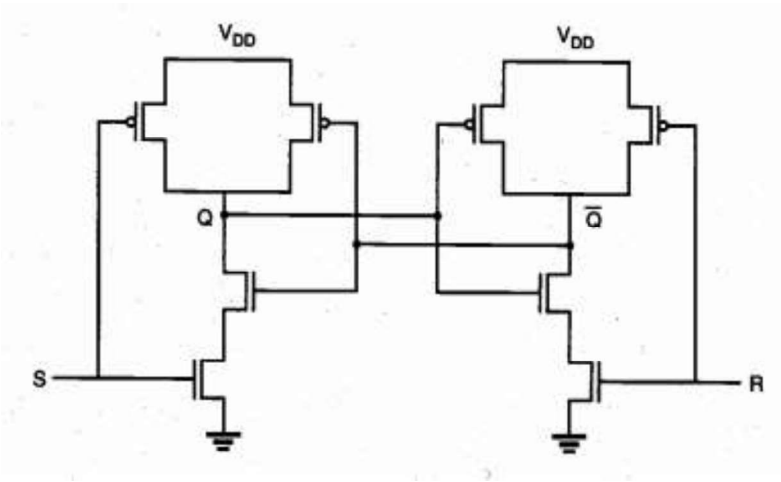


NAND SR latch responds to active low input signals whereas NOR SR latch responds to active high input signals.

Depletion load nMOS SR latch



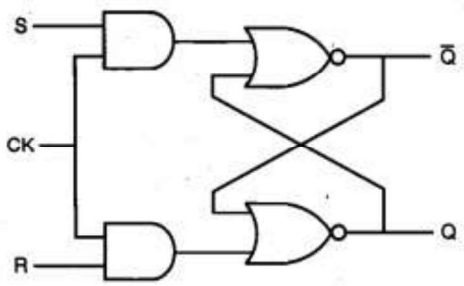
CMOS SR Latch circuit based on NOR2 gate



CMOS SR Latch circuit based on NAND 2 gate

CLOCKED LATCH AND FLIPFLOP CIRCUITS

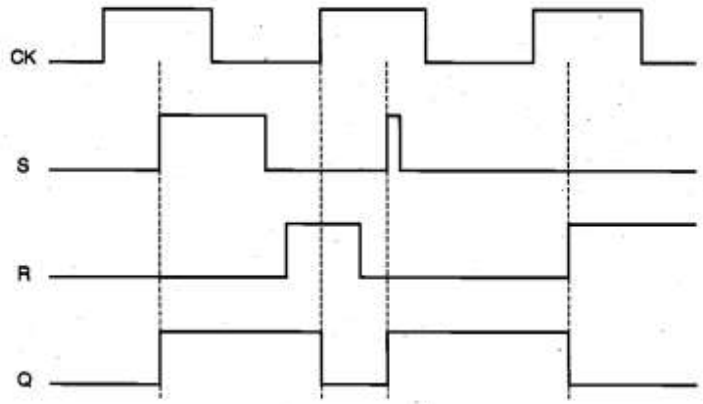
CLOCKED SR LATCH

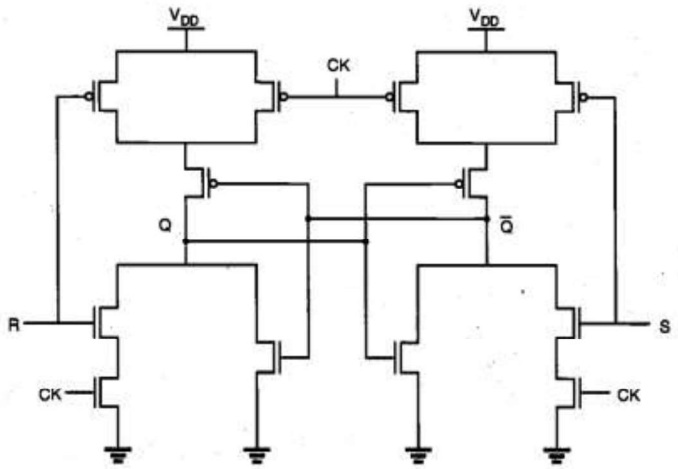


- Asynchronous sequential circuits, which will respond to the changes occurring in input signals at a circuit-delay-dependent time point during their operation.

- To facilitate synchronous operation, the circuit response can be controlled simply by adding a gating clock signal to the circuit, so that the outputs will respond to the input levels only during the active period of a clock pulse.

- It can be seen that if the clock (CK) is equal to logic "0," the input signals have no influence upon the circuit response.
- When the clock input goes to logic " 1," the logic levels applied to the S and R inputs are permitted to reach the SR latch, and possibly change its state.
- the circuit is strictly level-sensitive during active clock phases, i.e., any changes occurring. in the S and R input voltages when the CK level is equal to " 1 " will be reflected onto the circuit outputs.



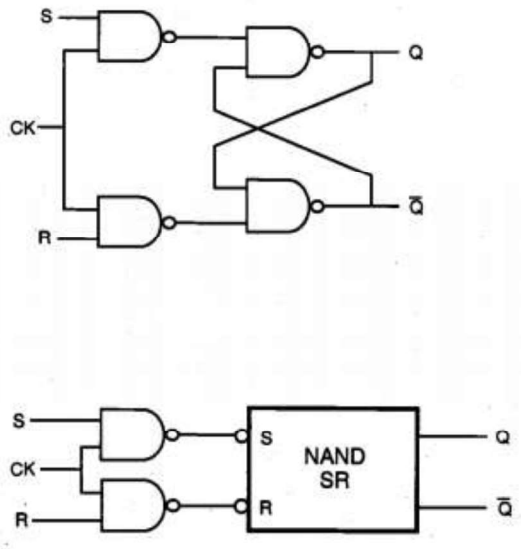


Sample input and output waveforms illustrating the operation of the clocked NOR based SR latch circuit.

clocked NOR-based SR latch circuit.

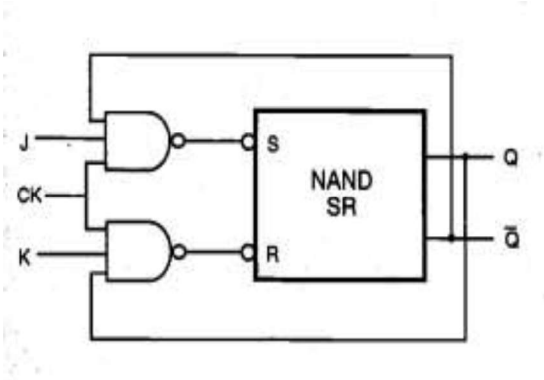
Both input signals S and R as well as the clock signal CK are active low in case of NAND.

NAND based SR latch

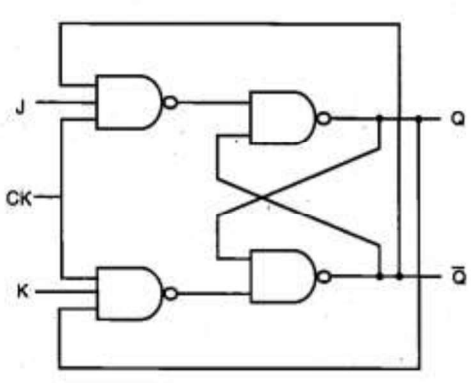


CLOCKED JK LATCH

- The J and K inputs in this circuit correspond to the set and reset inputs of the basic SR latch.
- When the clock is active, the latch can be set with the input combination (J = '1," K = "0"), and it can be reset with the input combination (J = "0," K = "1").
- If both inputs are equal to logic "0," the latch preserves its current state.
- If, on the other hand, both inputs are equal to " 1 " during the active clock phase, the latch simply switches its state due to feedback.



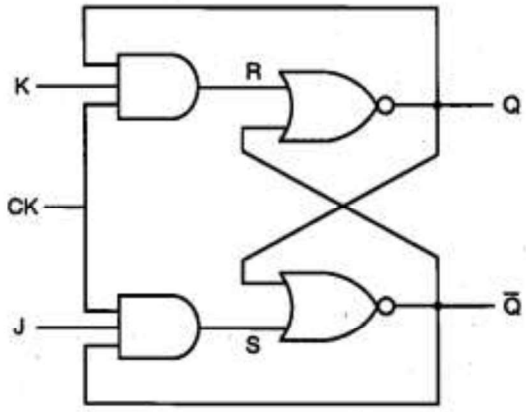
Gate level schematic of the clocked NAND – based JK Latch



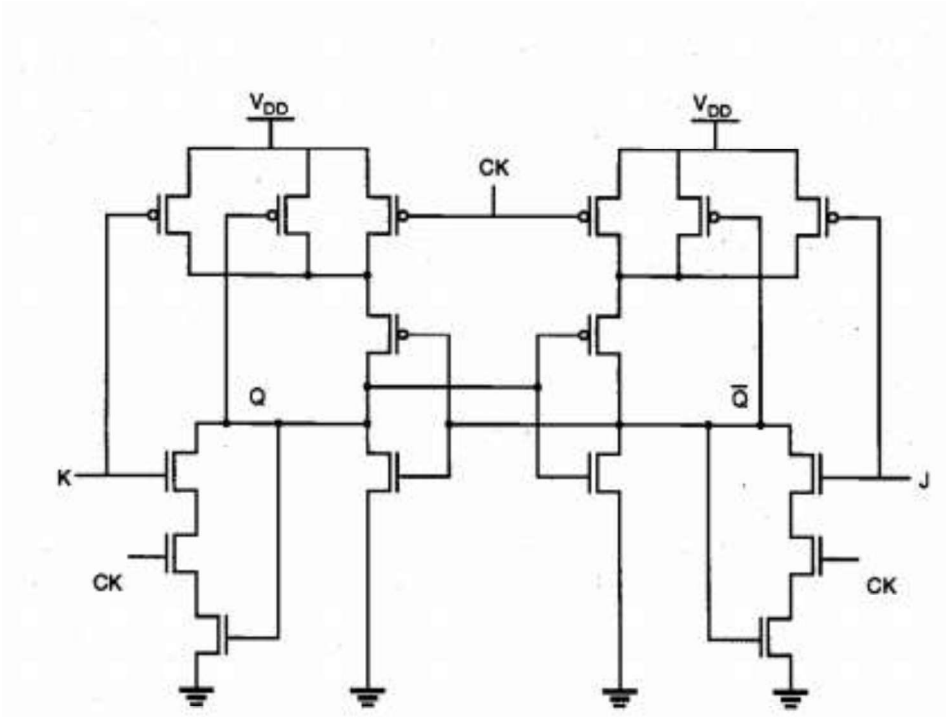
All NAND implementation of the clocked JK latch circuit

Detailed truth table of the JK Latch circuit

J	K	Q_n	$\overline{Q}_n$	S	R	Q_{n+1}	$\overline{Q_{n+1}}$	Operati-on
0	0	0 1	1 0	1 1	1 1	0 1	1 0	hold
0	1	0 1	1 0	1 1	1 0	0 0	1 1	reset
1	0	0 1	1 0	0 1	1 1	1 1	0 0	set
1	1	0 1	1 0	0 1	1 0	1 0	0 1	toggle



a) Gate level schematic of the clocked NOR based JK Latch



b) CMOS realization of the JK Latch

NOTE:

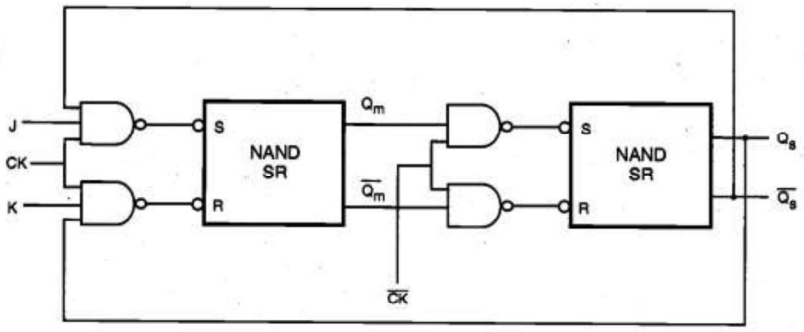
- If both inputs are equal to logic " 1 " during the active phase of the clock pulse, the output of the circuit will oscillate (toggle) continuously until either the clock becomes inactive (goes to zero), or one of the input signals goes to zero.
- To prevent this undesirable timing problem, the clock pulse width must be made smaller than the input-to-output propagation delay of the JK latch circuit.
- This restriction dictates that the clock signal must go low before the output level has an opportunity to switch again, which prevents uncontrolled oscillation of the output.

MASTER SLAVE FLIP-FLOP

operating principle: the two cascaded stages are activated with opposite clock phases.

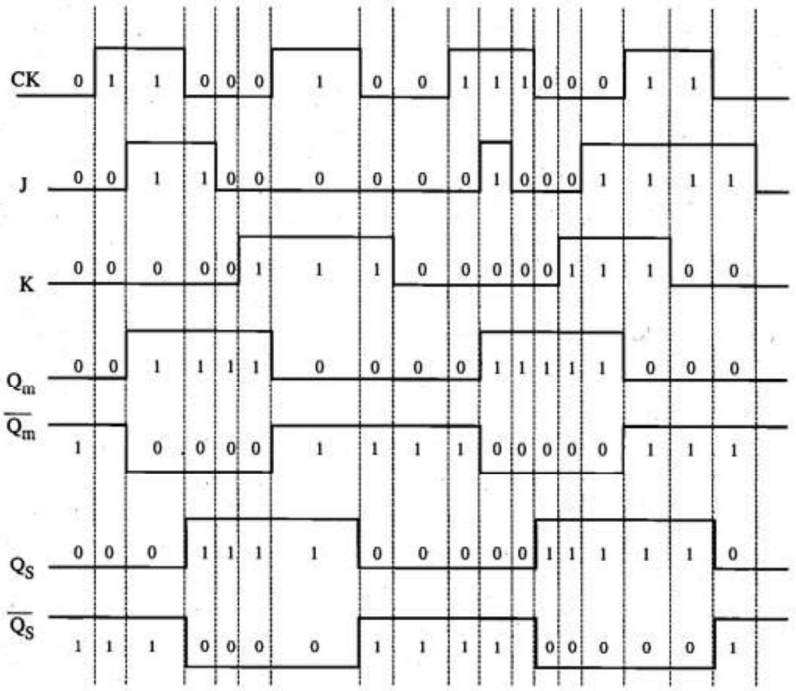
WORKING:

- The input latch in called the "master," is activated when the clock pulse is high. During this phase, the inputs J and K allow data to be entered into the flip-flop, and the first-stage outputs are set according to the primary inputs.
- When the clock pulse goes to zero, the master latch becomes inactive and the second-stage latch, called the "slave," becomes active. The output levels of the flip-flop circuit are determined during this second phase, based on the master-stage outputs set in the previous phase.



Master slave flip flop consisting of NAND based JK Latches.

- The circuit is never transparent, i.e., a change occurring in the primary inputs is never reflected directly to the outputs.
- Eliminates the possibility of uncontrolled oscillations since only one stage is active at any given time.
- Has the potential problem of " 1's catching." When the clock pulse is high, a narrow glitch in one of the inputs, for instance a glitch in the J line (or K line), may set (or reset) the master latch and thus cause an unwanted state transition, which will then be propagated into the slave stage during the following phase.



Input and output waveforms of the master-slave flip-flop