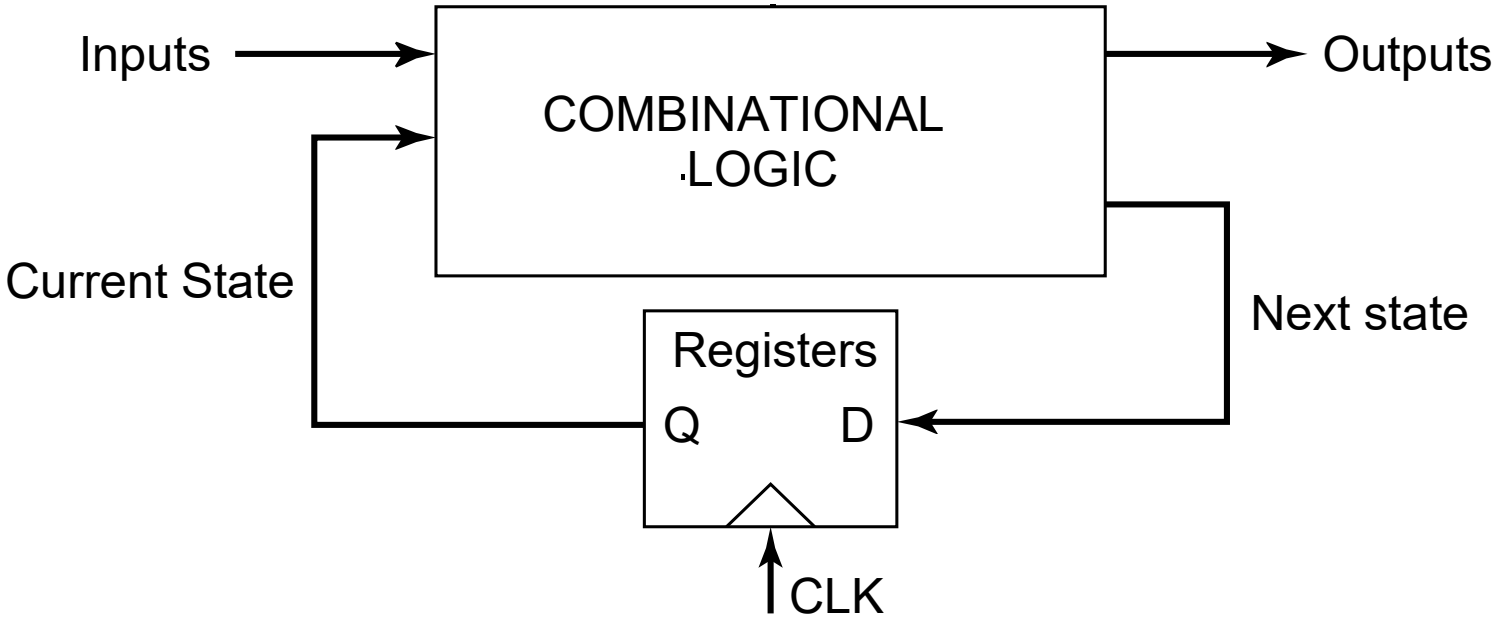
Sequential Logic



2 storage mechanisms

- **positive feedback**
- **charge-based**

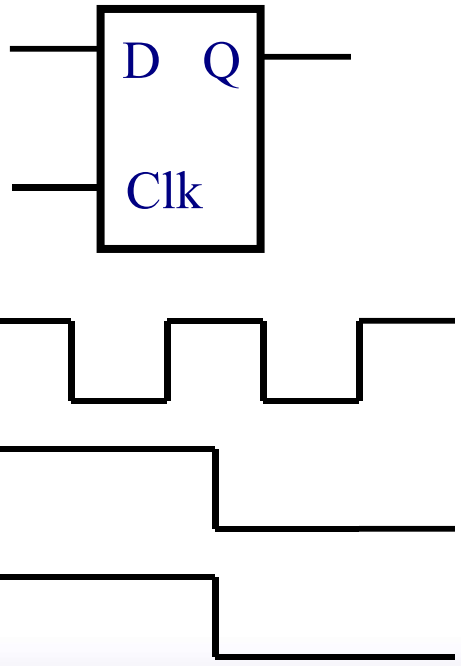
Naming Conventions

- In our text:
  - a latch is level sensitive
  - a register is edge-triggered
- There are many different naming conventions
  - For instance, many books call edge-triggered elements flip-flops
  - This leads to confusion however

Latch versus Register

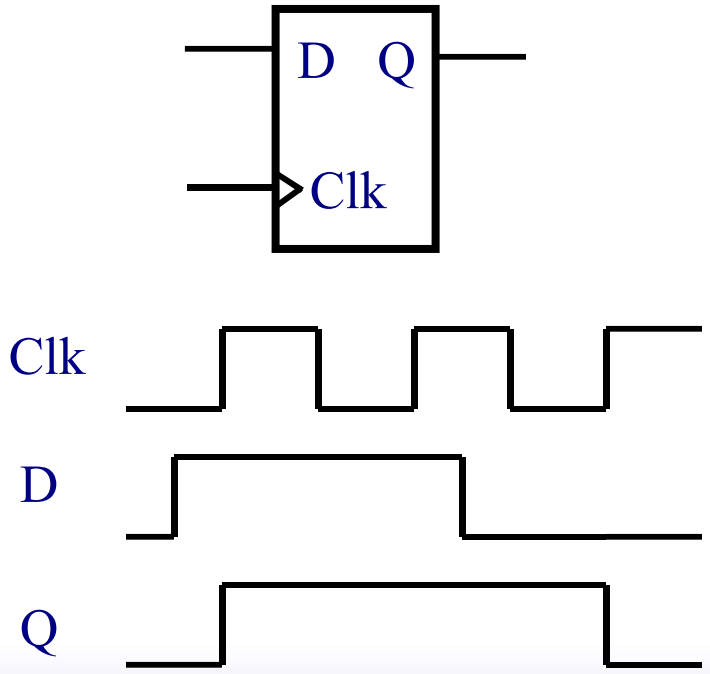
- Latch

  stores data when clock is low

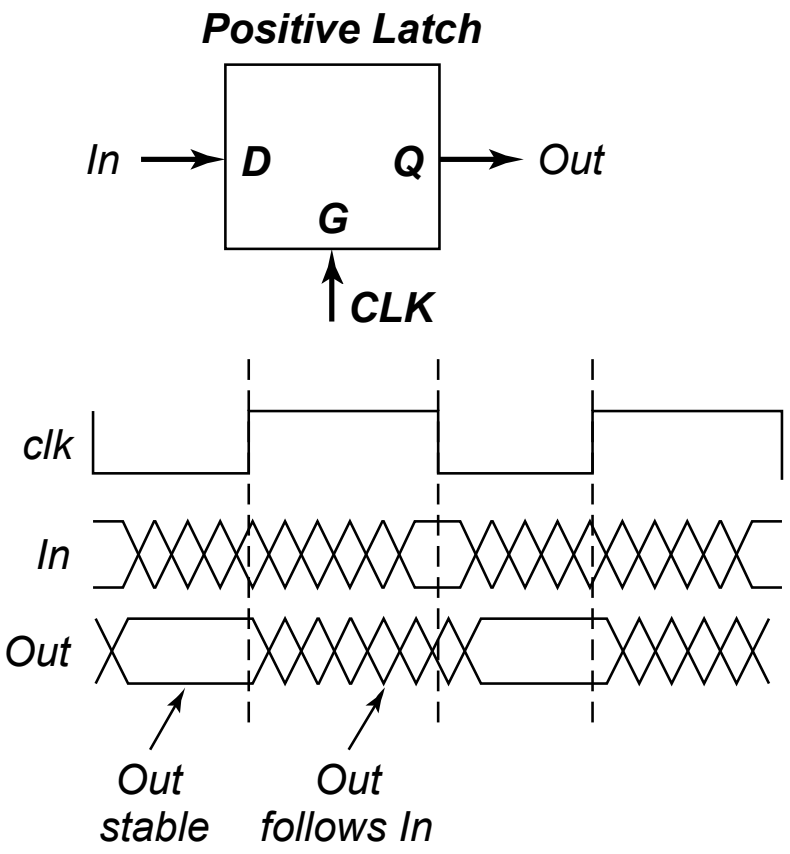


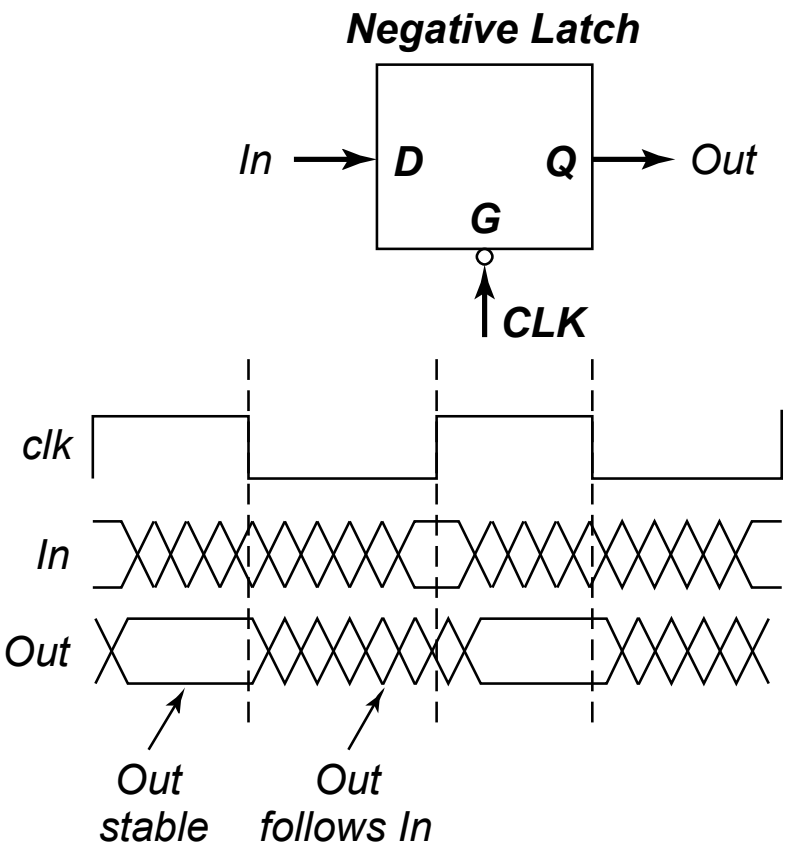
- Register

  stores data when clock rises



Latches

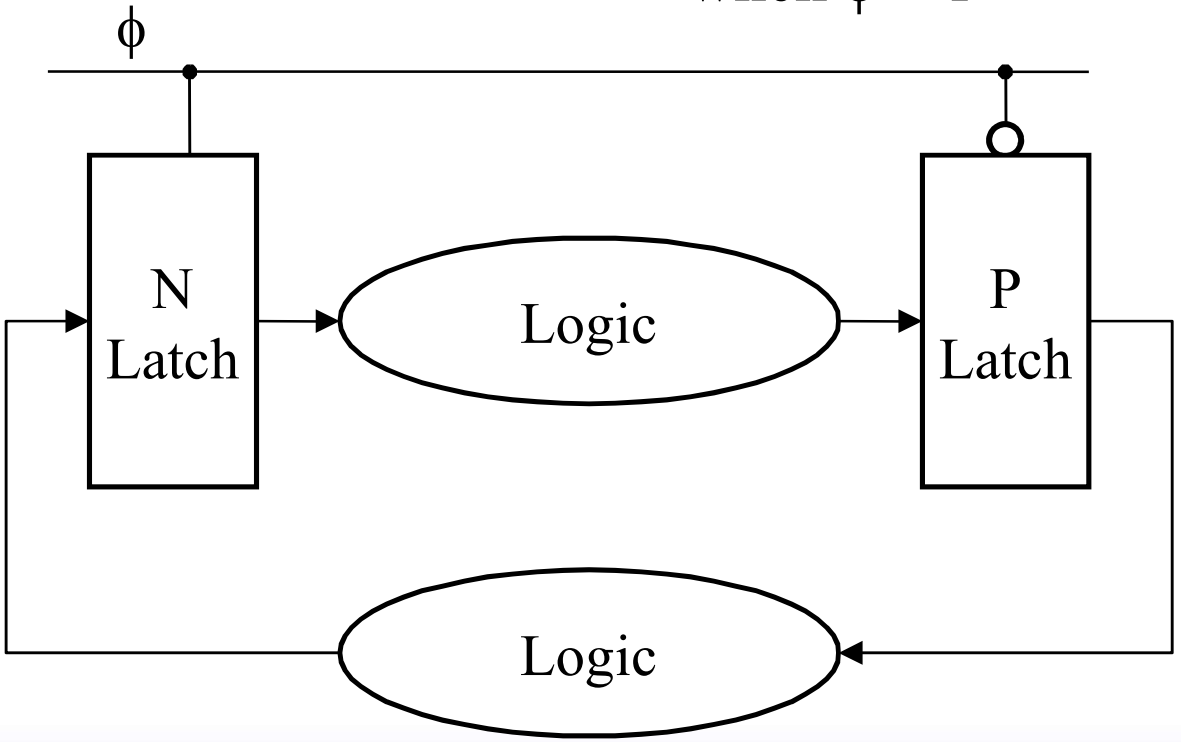

Positive Latch
In
D
Q
Out
G
CLK
clk
In
Out
Out stable
Out follows In


Negative Latch
In
D
Q
Out
G
CLK
clk
In
Out
Out stable
Out follows In

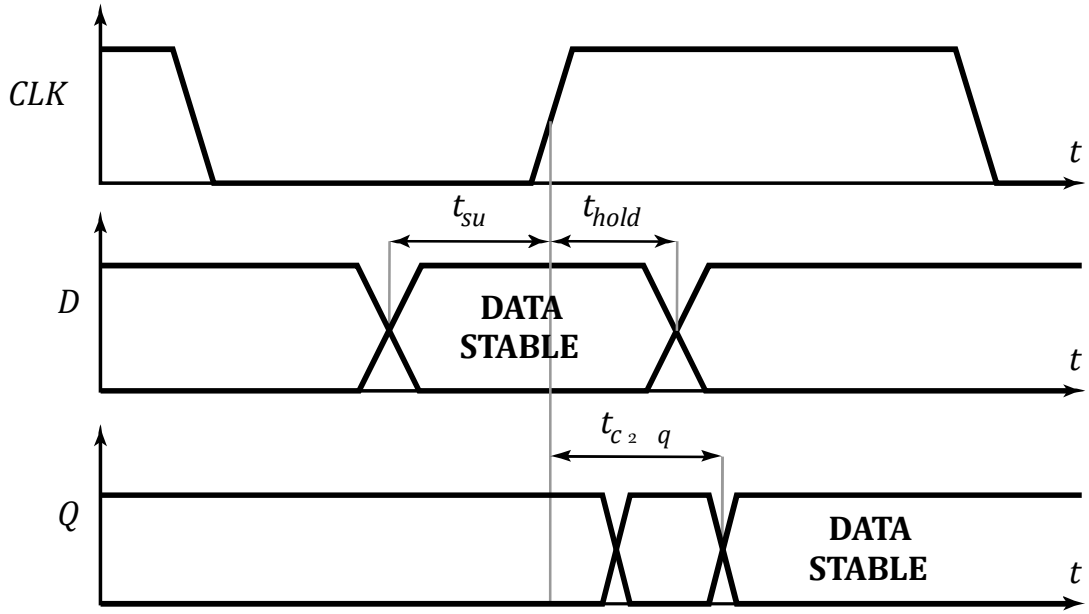
Latch-Based Design

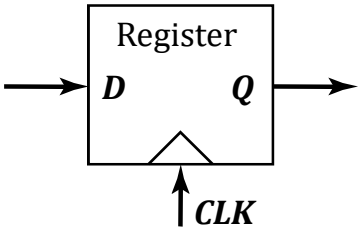
• N latch is transparent when $\phi = 0$

• P latch is transparent when $\phi = 1$

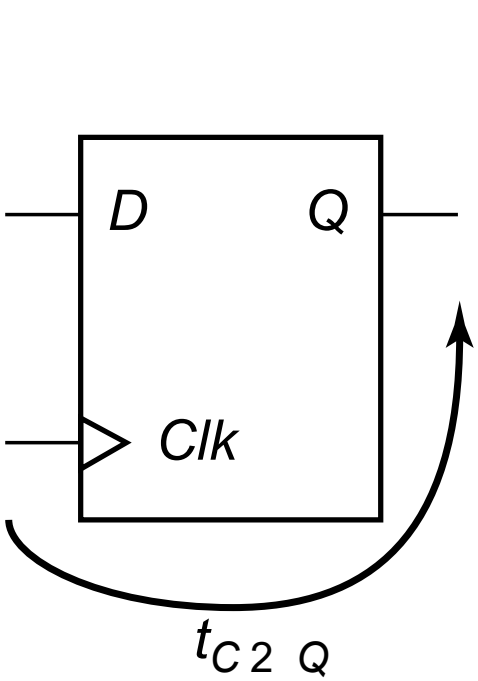


Timing Definitions

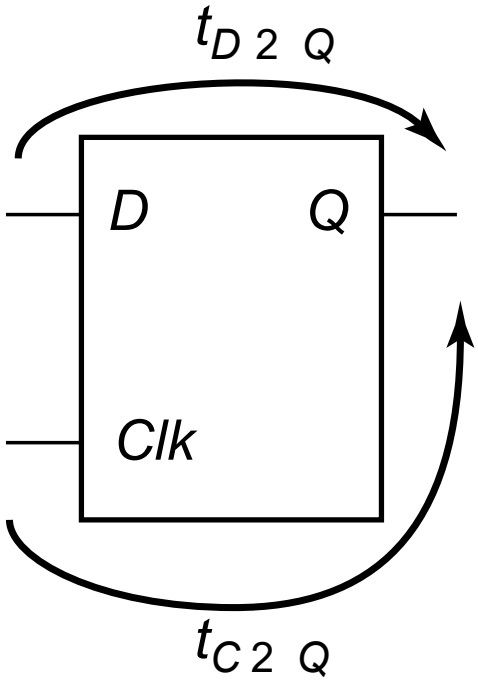




Characterizing Timing

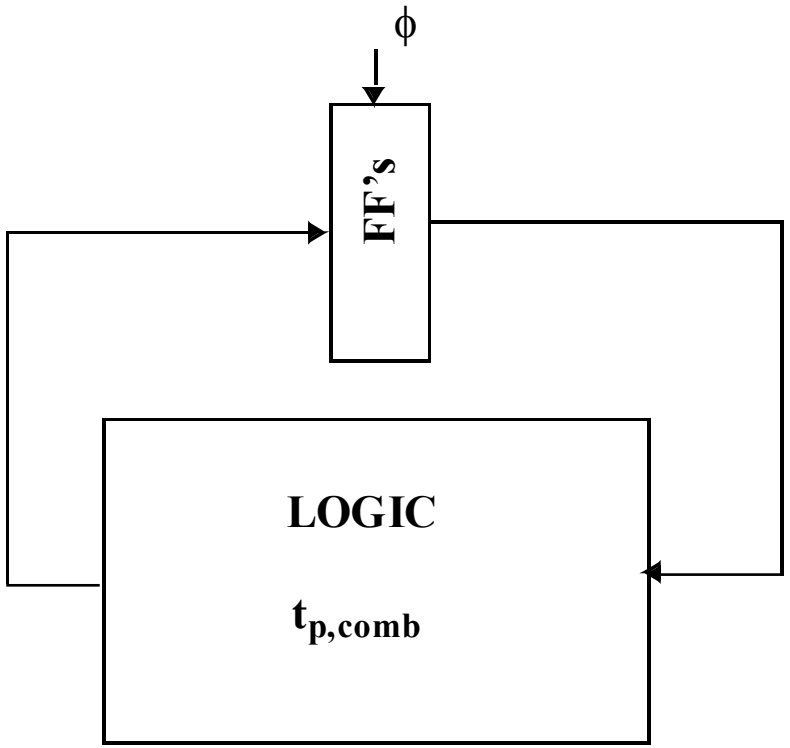


Register



Latch

Maximum Clock Frequency



$t_{clk\text{-}Q} + t_{p,comb} + t_{setup} = T$

Also:

$t_{cdreg} + t_{cdlogic} > t_{hold}$

t_{cd}: contamination delay = minimum delay