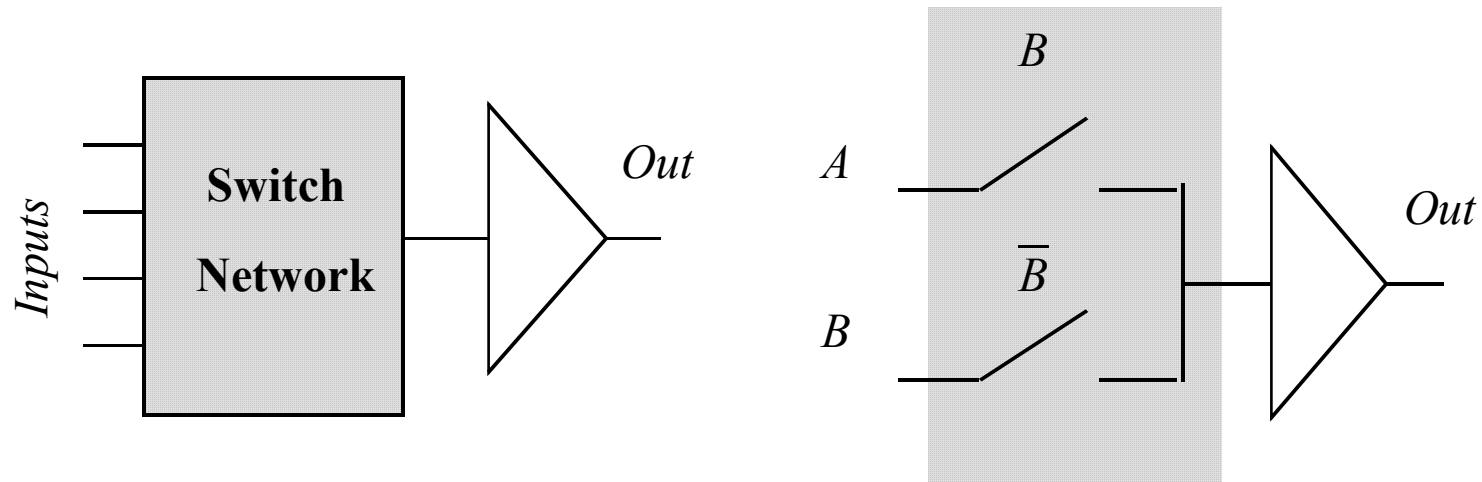


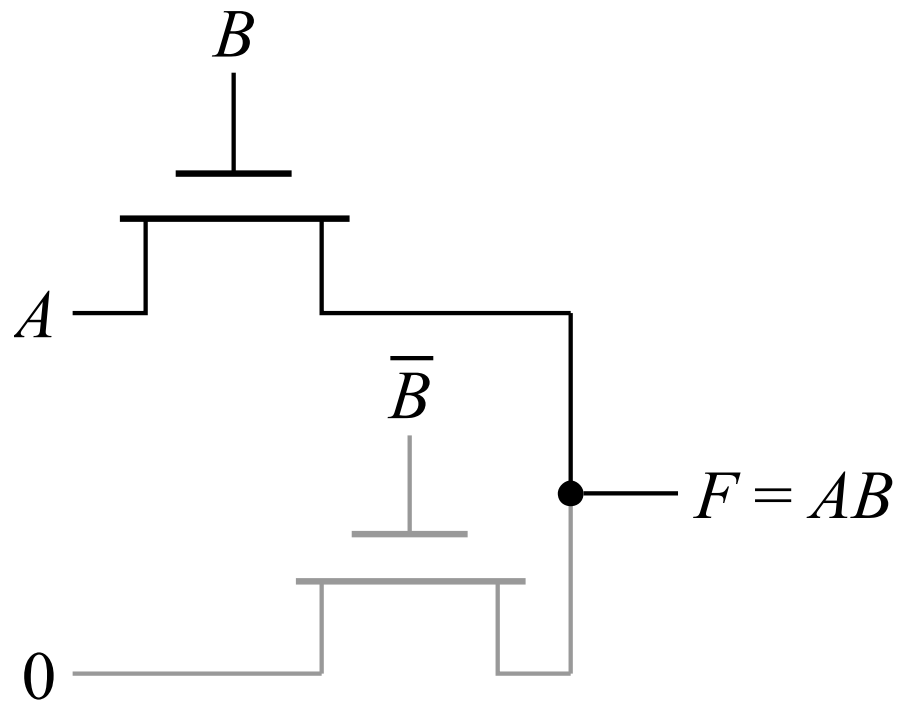
Pass-Transistor Logic

Pass-Transistor Logic

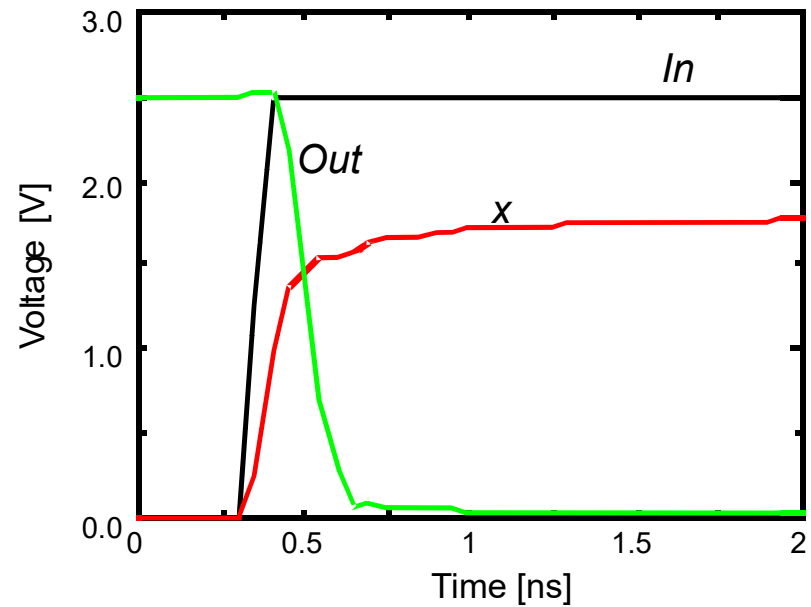
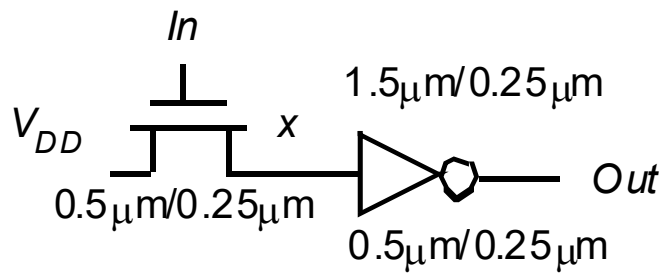


- **N transistors**
- **No static consumption**

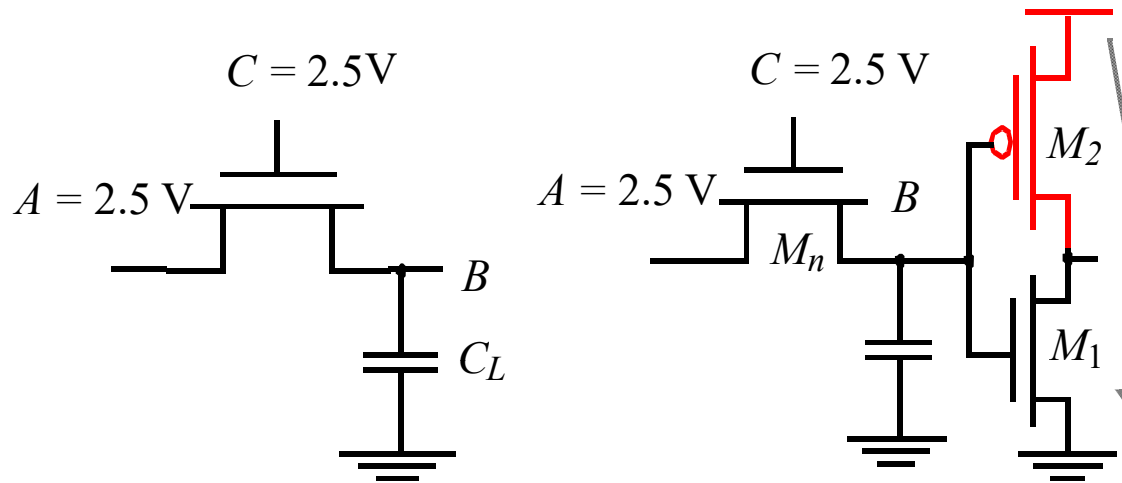
Example: AND Gate



NMOS-Only Logic



NMOS-only Switch

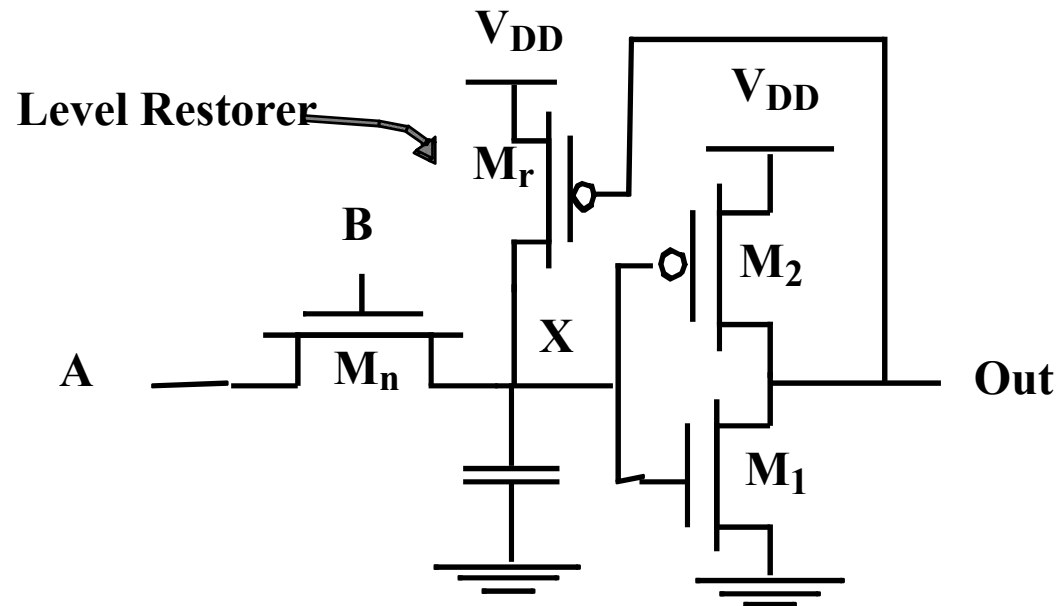


V_B does not pull up to 2.5V, but $2.5V - V_{TN}$

Threshold voltage loss causes
static power consumption

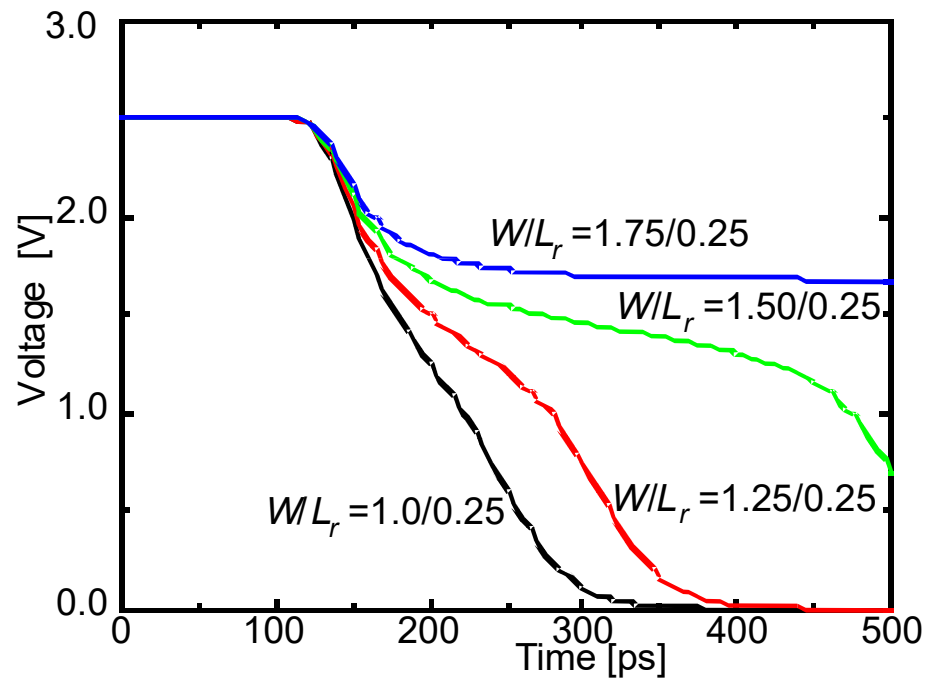
NMOS has higher threshold than PMOS (body effect)

NMOS Only Logic: Level Restoring Transistor



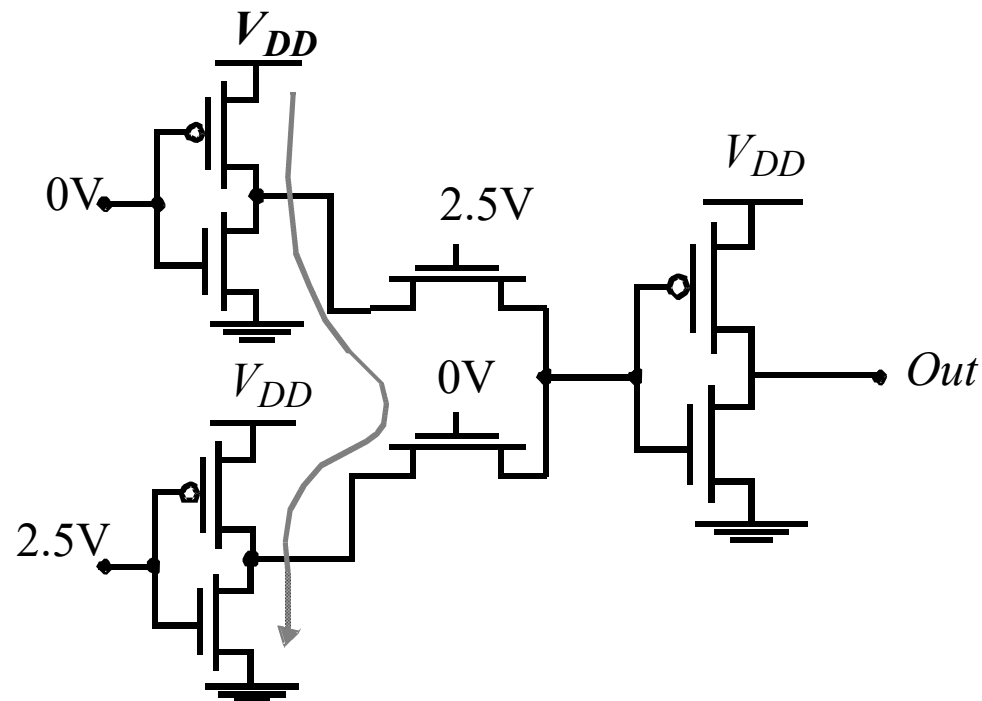
- Advantage: Full Swing
- Restorer adds capacitance, takes away pull down current at X
- Ratio problem

Restorer Sizing



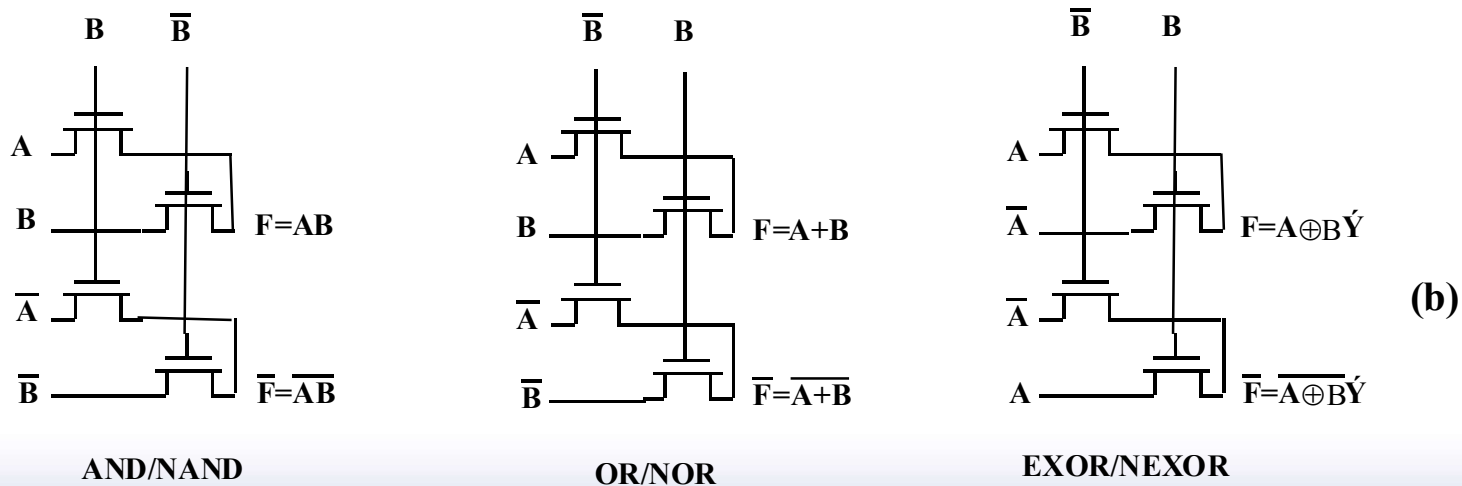
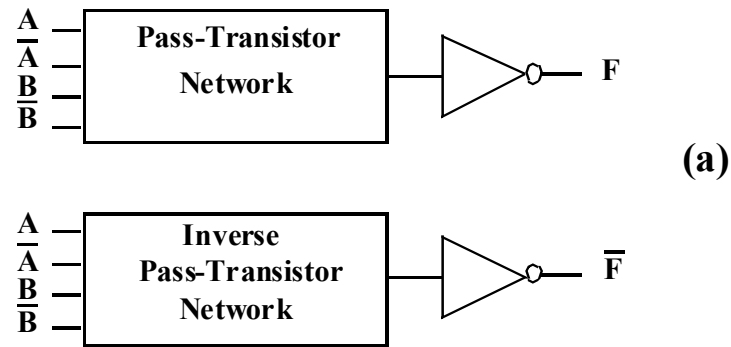
- Upper limit on restorer size
- Pass-transistor pull-down can have several transistors in stack

Solution 2: Single Transistor Pass Gate with $V_T=0$

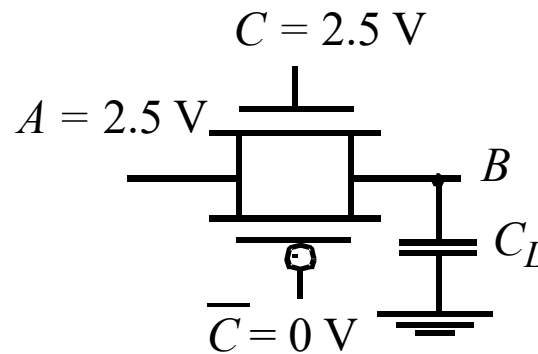
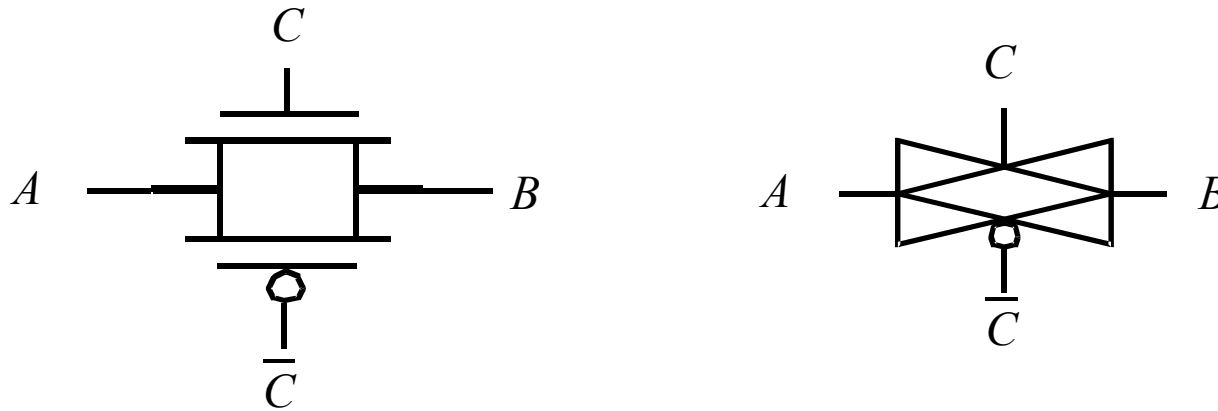


WATCH OUT FOR LEAKAGE CURRENTS

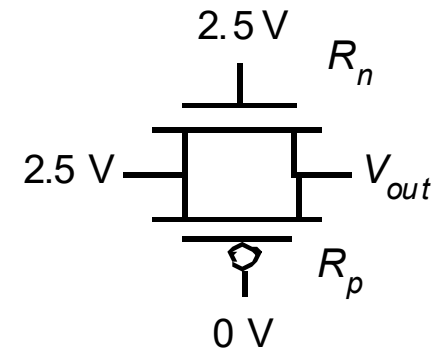
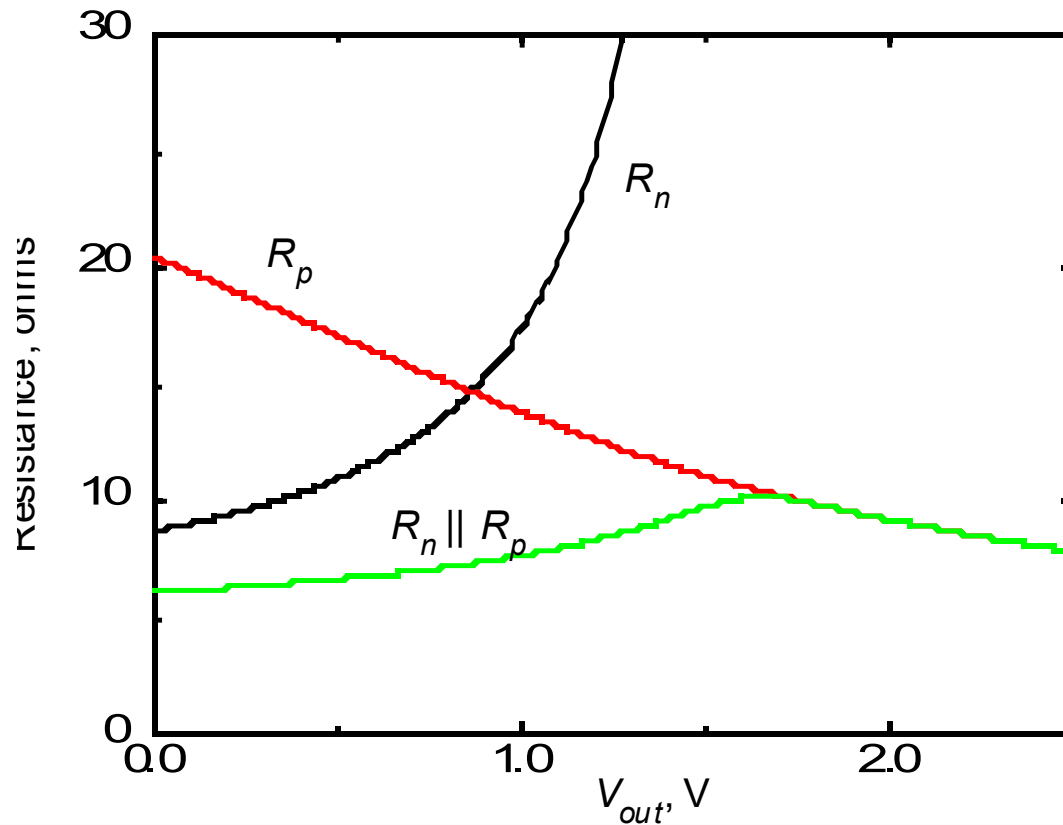
Complementary Pass Transistor Logic



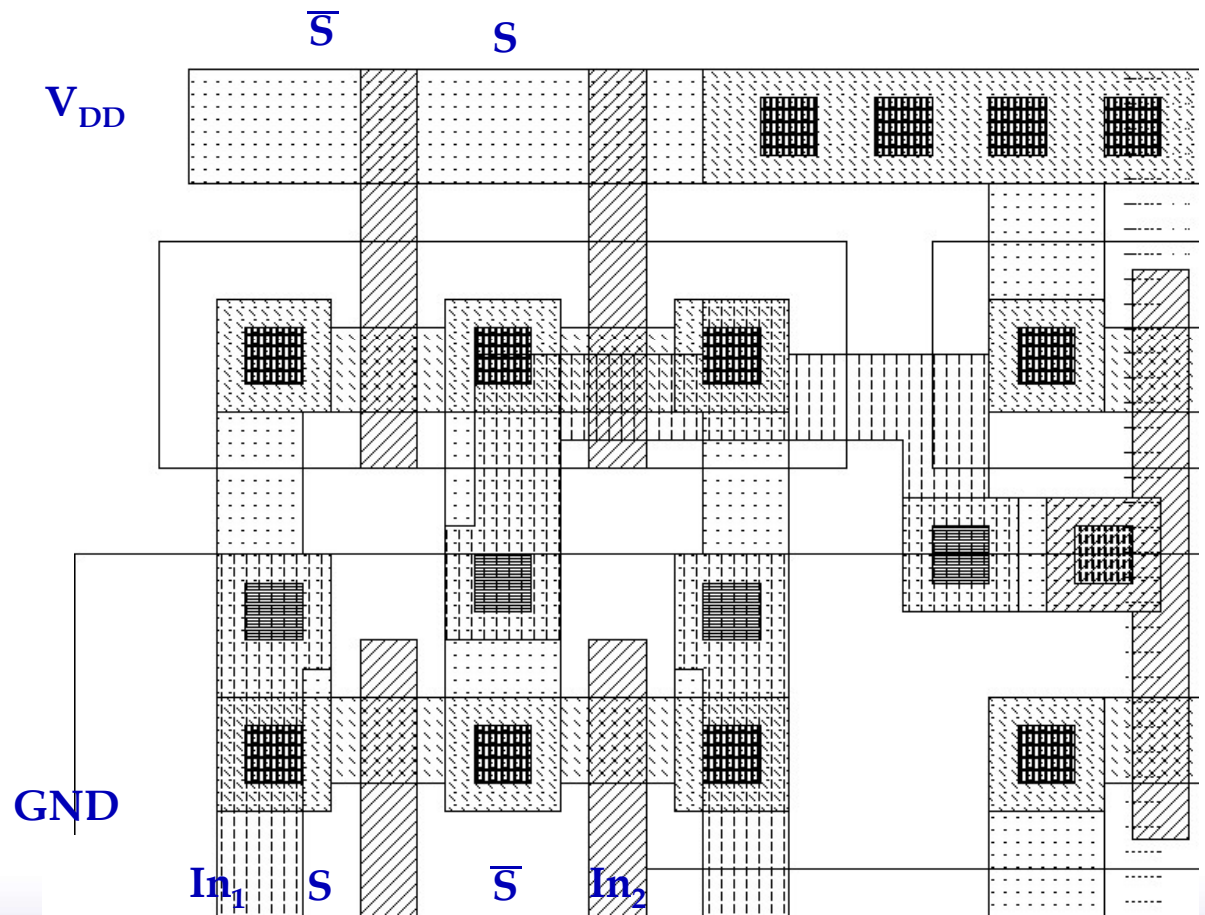
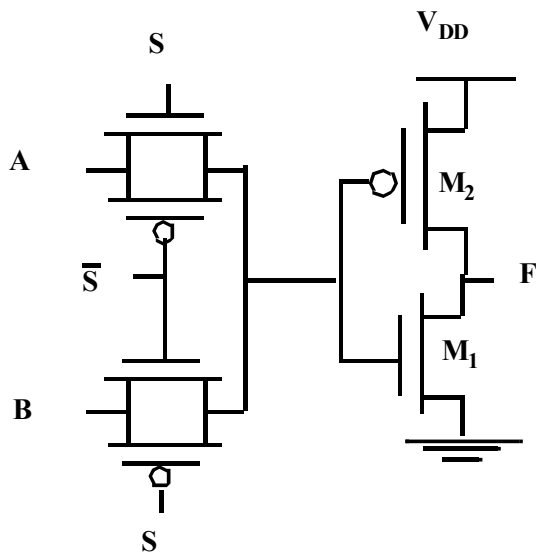
Solution 3: Transmission Gate



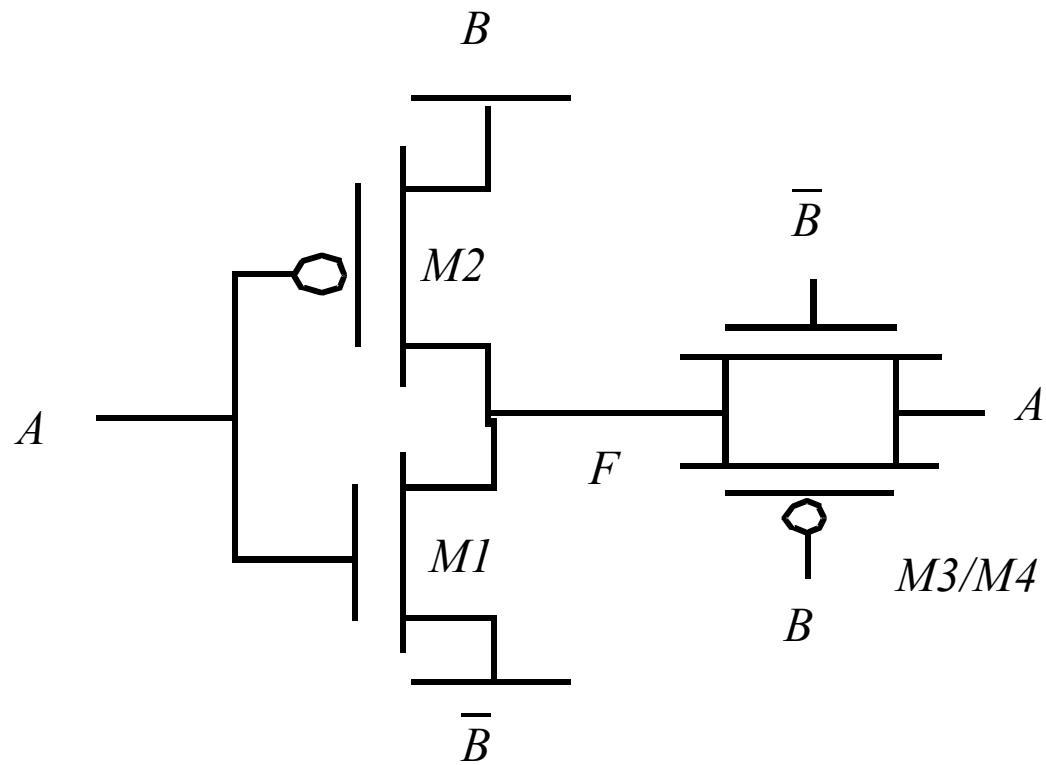
Resistance of Transmission Gate



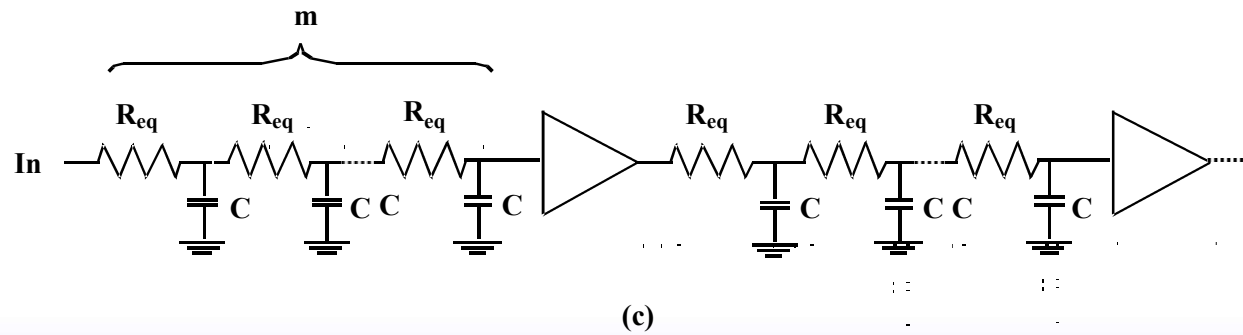
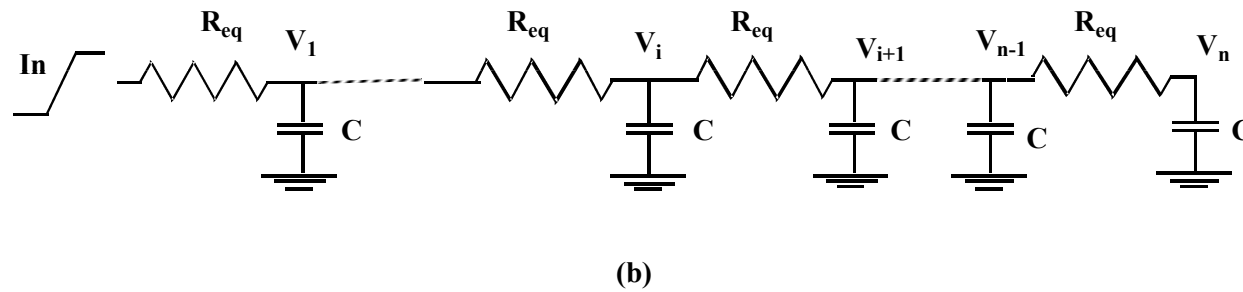
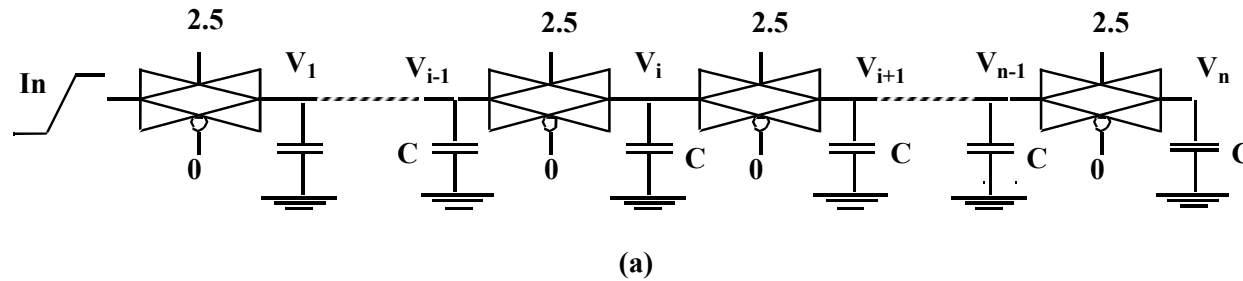
Pass-Transistor Based Multiplexer



Transmission Gate XOR



Delay in Transmission Gate Networks



Delay Optimization

- Delay of RC chain

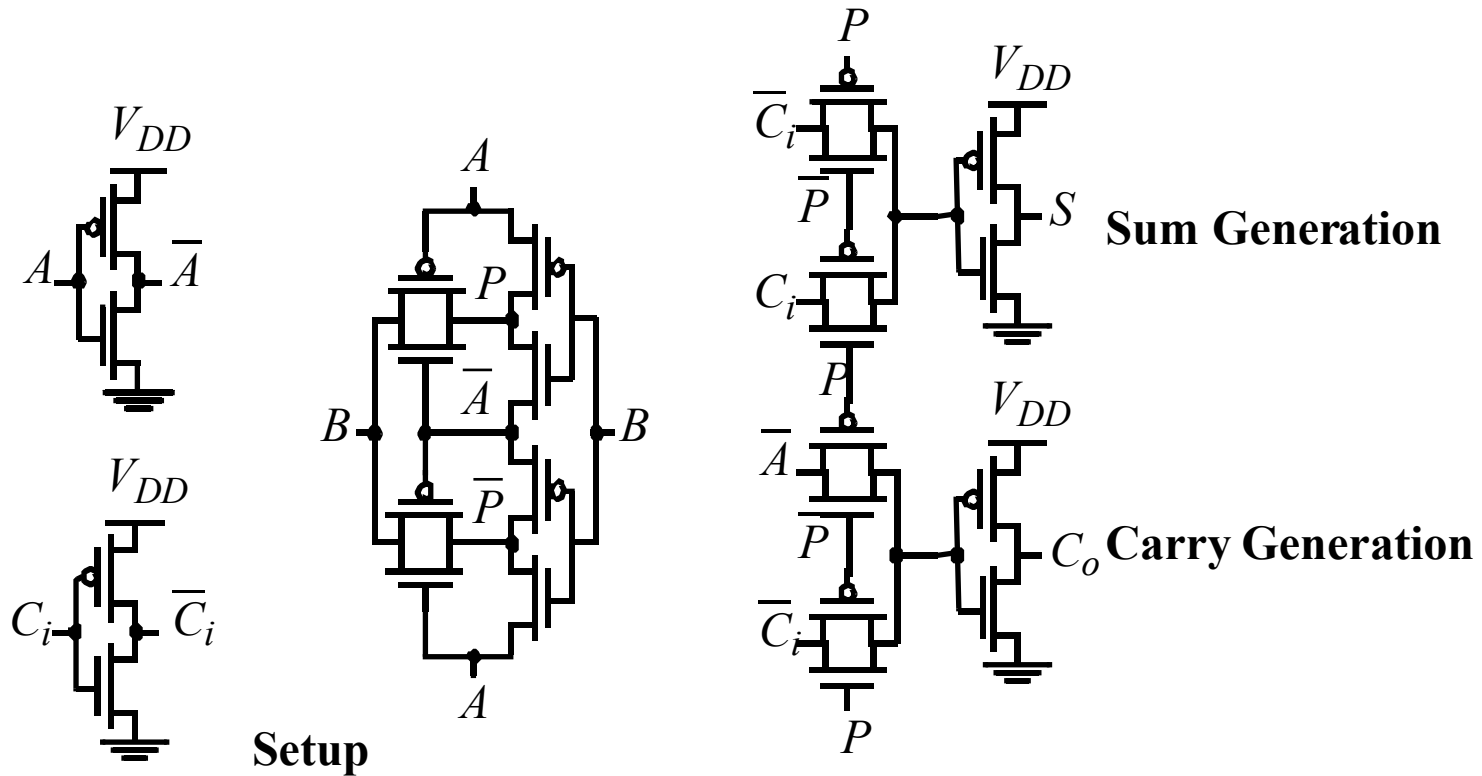
$$t_p = 0.69 \sum_{k=0}^n CR_{eq}^k = 0.69 CR_{eq} \frac{n(n+1)}{2}$$

- Delay of Buffered Chain

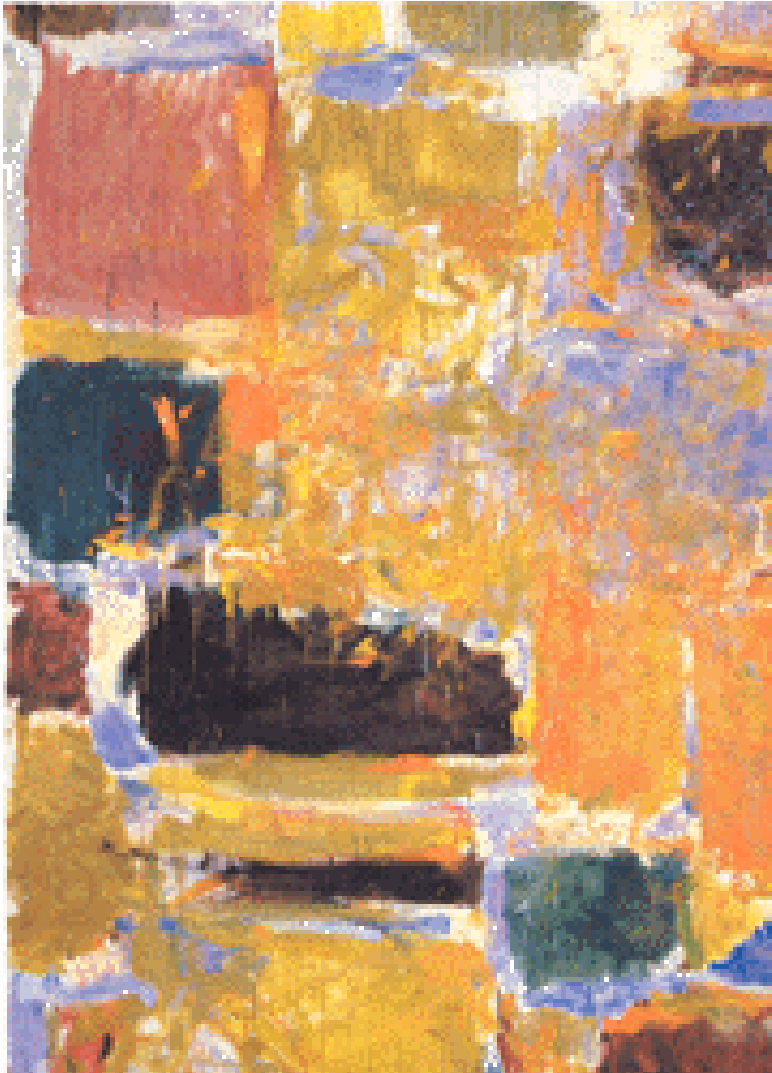
$$\begin{aligned} t_p &= 0.69 \left[\frac{n}{m} CR_{eq} \frac{m(m+1)}{2} \right] + \left(\frac{n}{m} - 1 \right) t_{buf} \\ &= 0.69 \left[CR_{eq} \frac{n(m+1)}{2} \right] + \left(\frac{n}{m} - 1 \right) t_{buf} \end{aligned}$$

$$m_{opt} = 1.7 \sqrt{\frac{t_{pbuf}}{CR_{eq}}}$$

Transmission Gate Full Adder

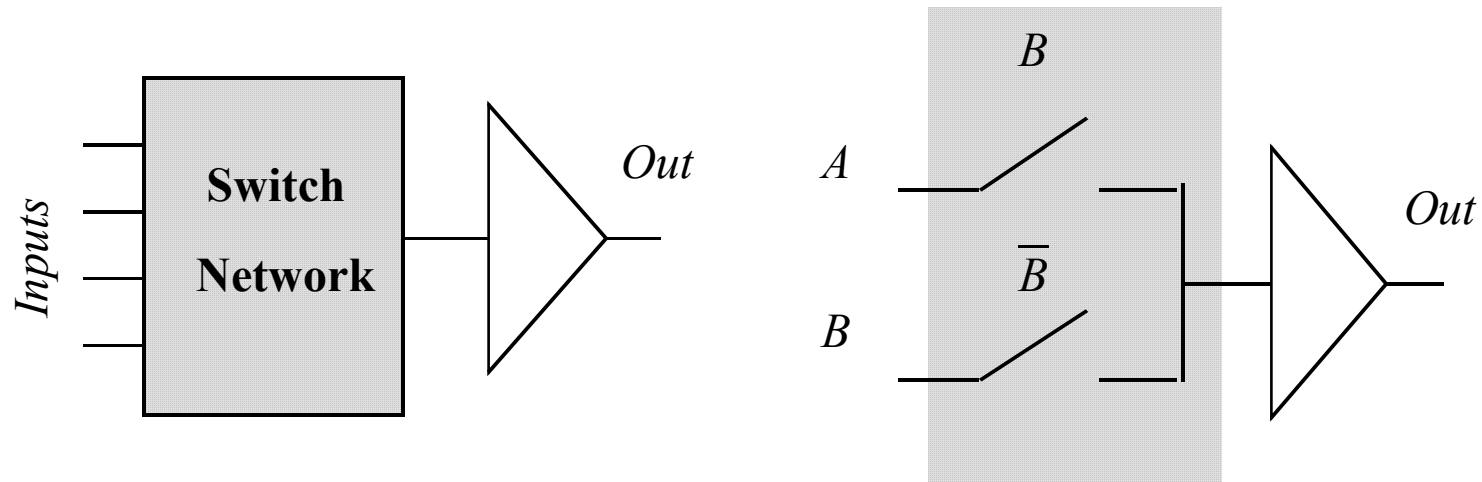


Similar delays for sum and carry



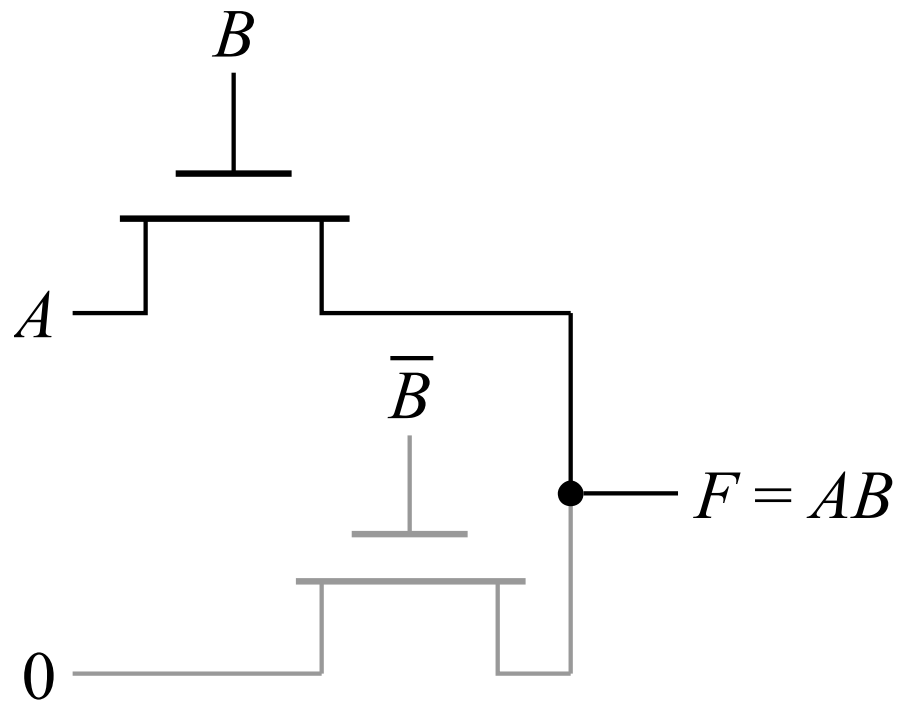
Pass-Transistor Logic

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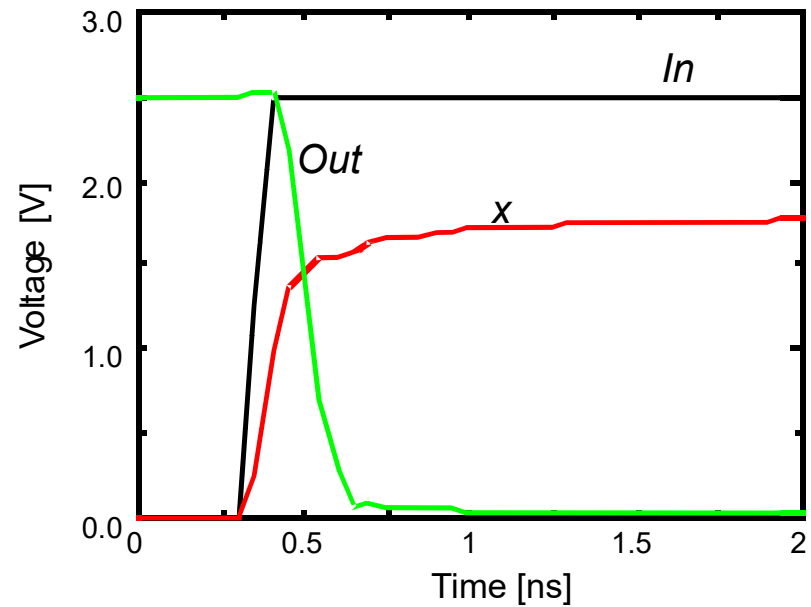
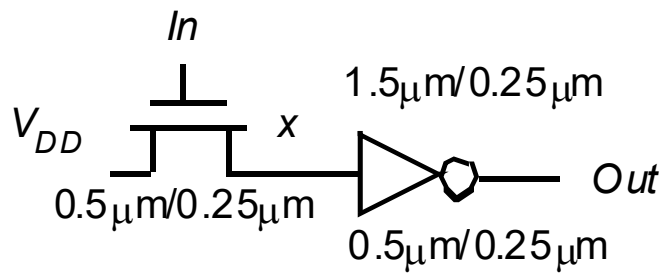


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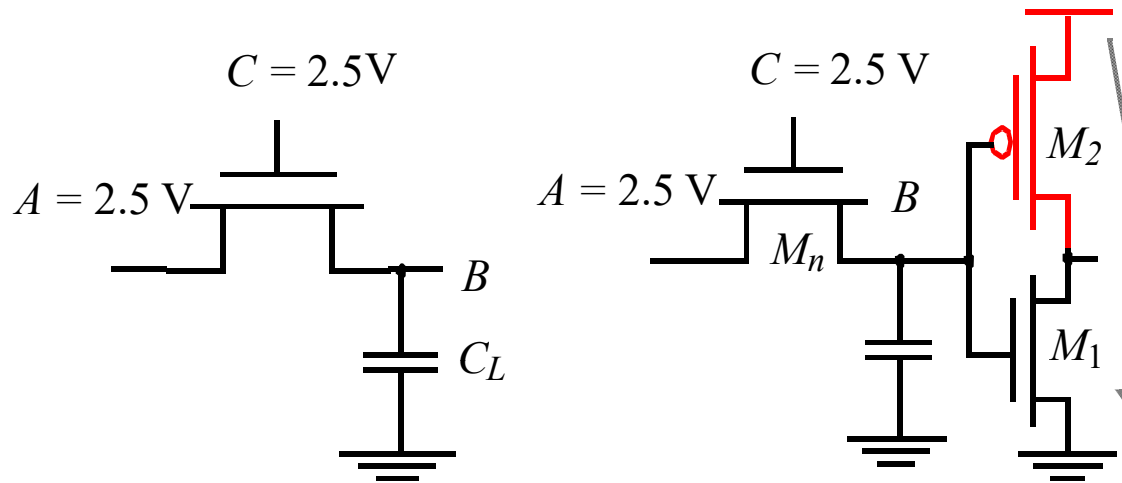
Example: AND Gate



NMOS-Only Logic



NMOS-only Switch

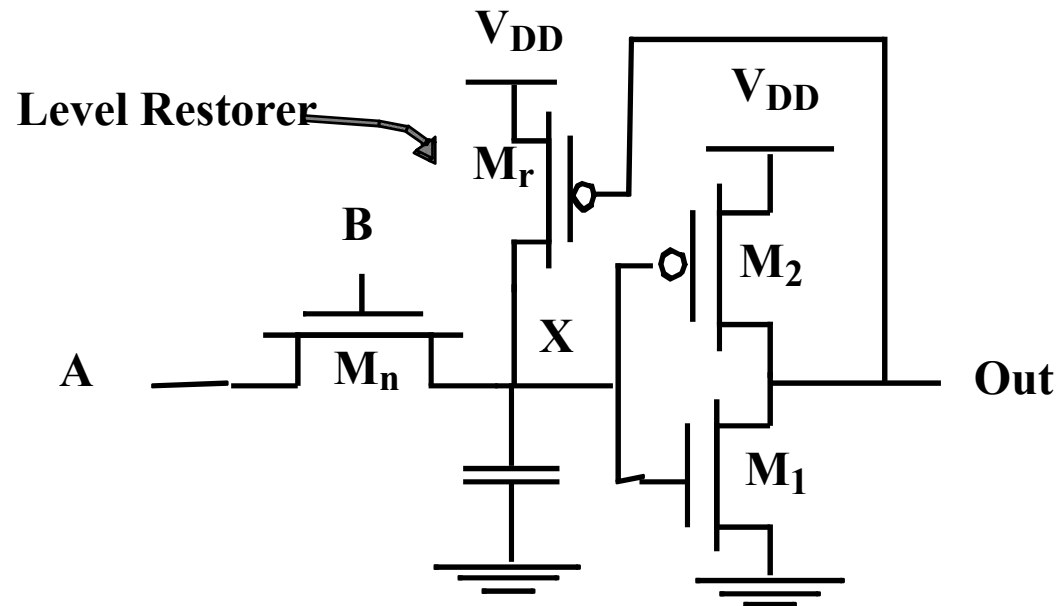


V_B does not pull up to 2.5V , but $2.5\text{V} - V_{TN}$

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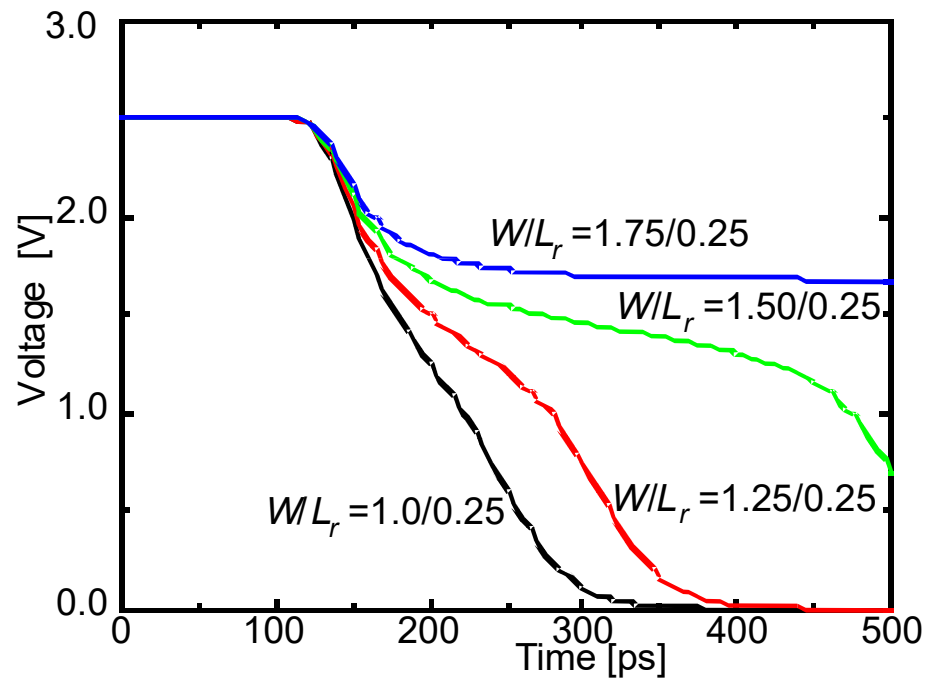
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NMOS Only Logic: Level Restoring Transistor



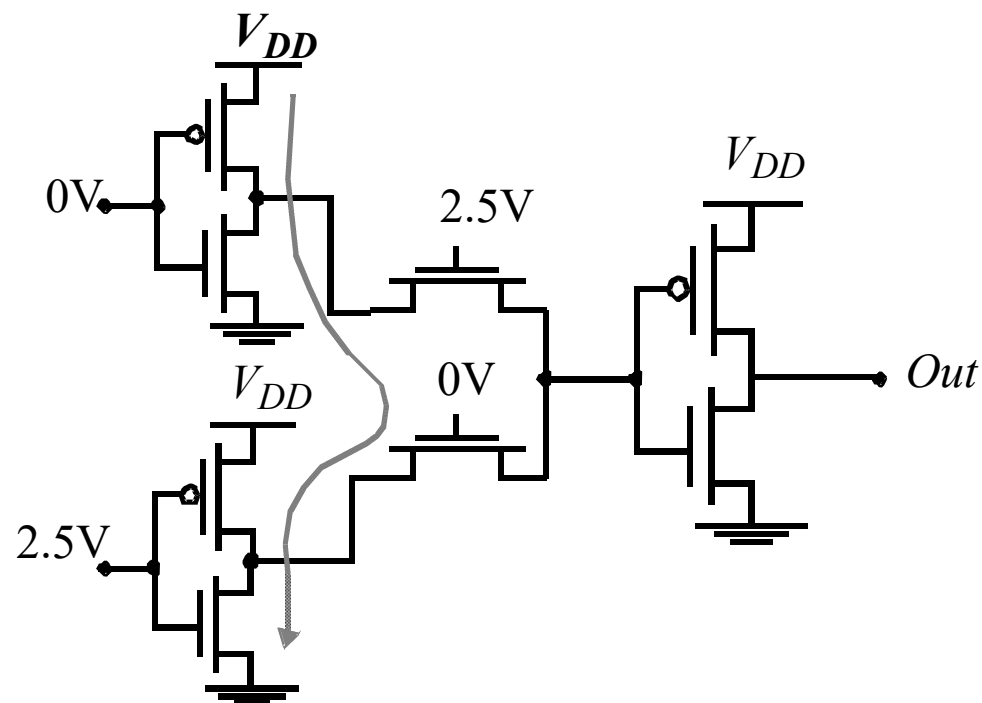
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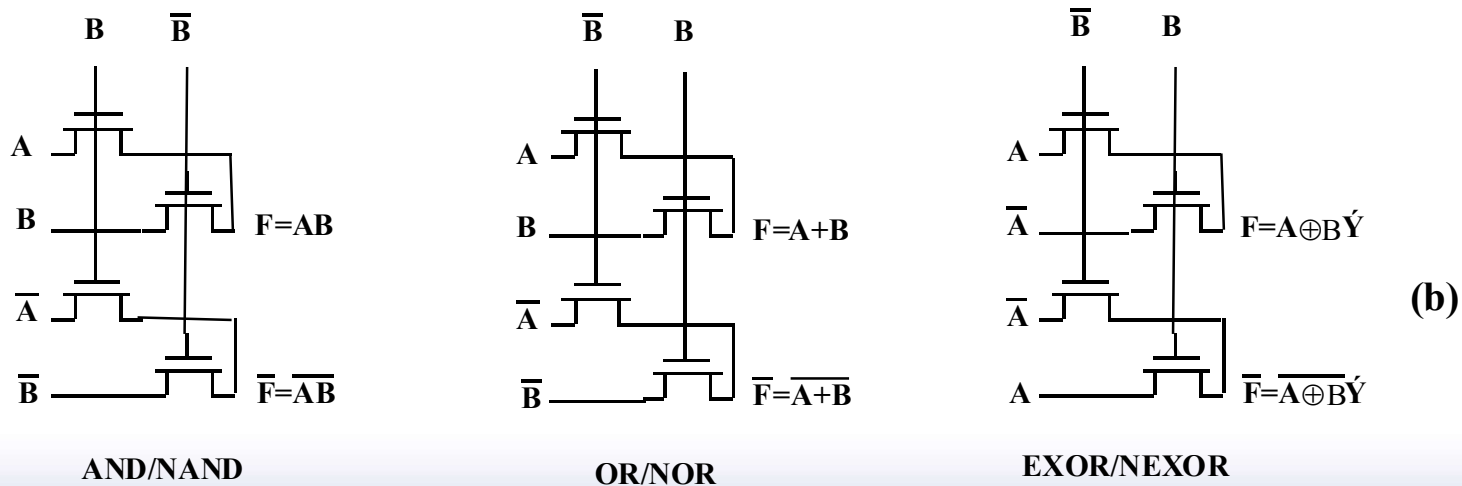
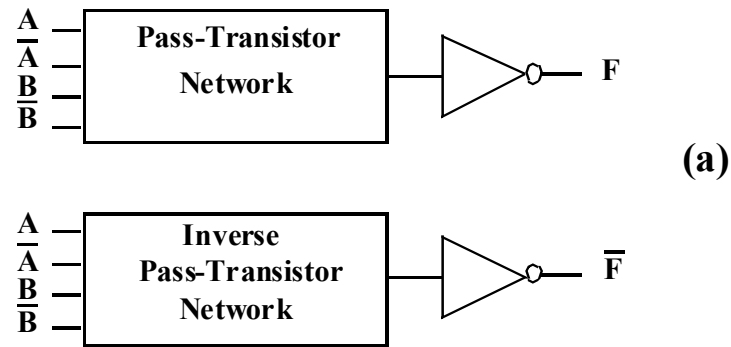
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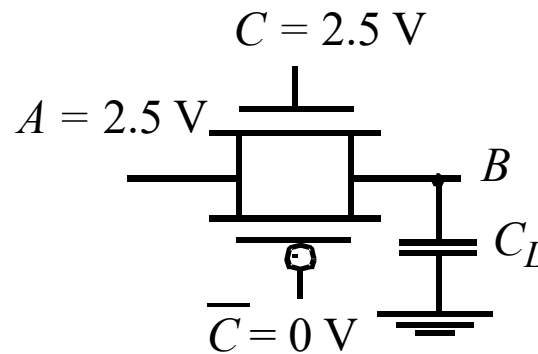
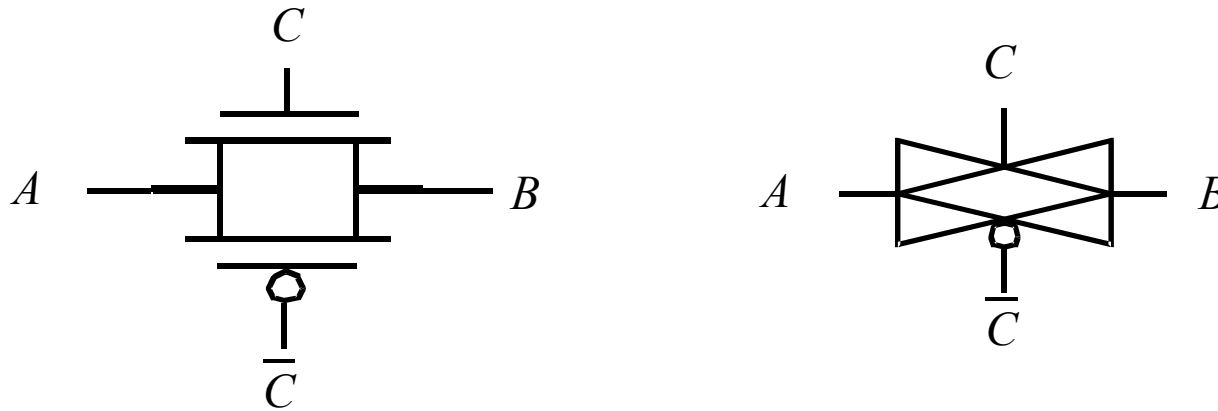


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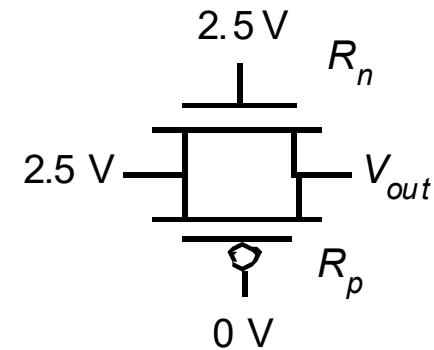
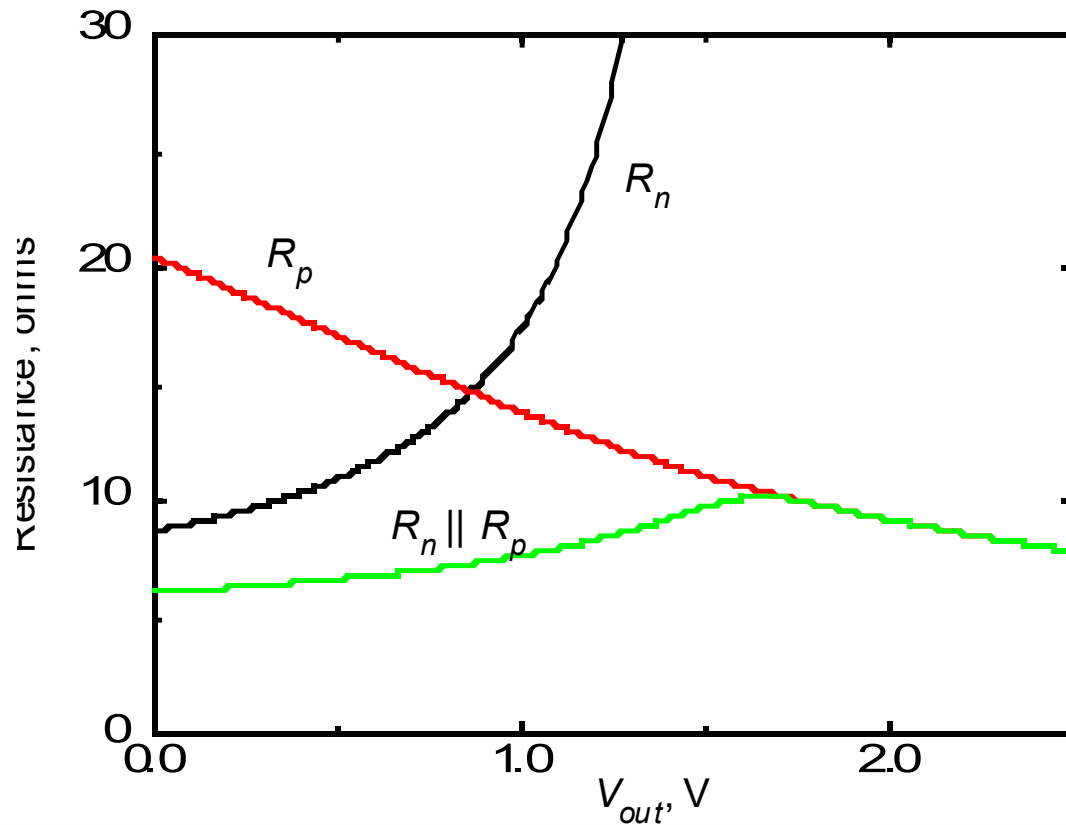
Complementary Pass Transistor Logic



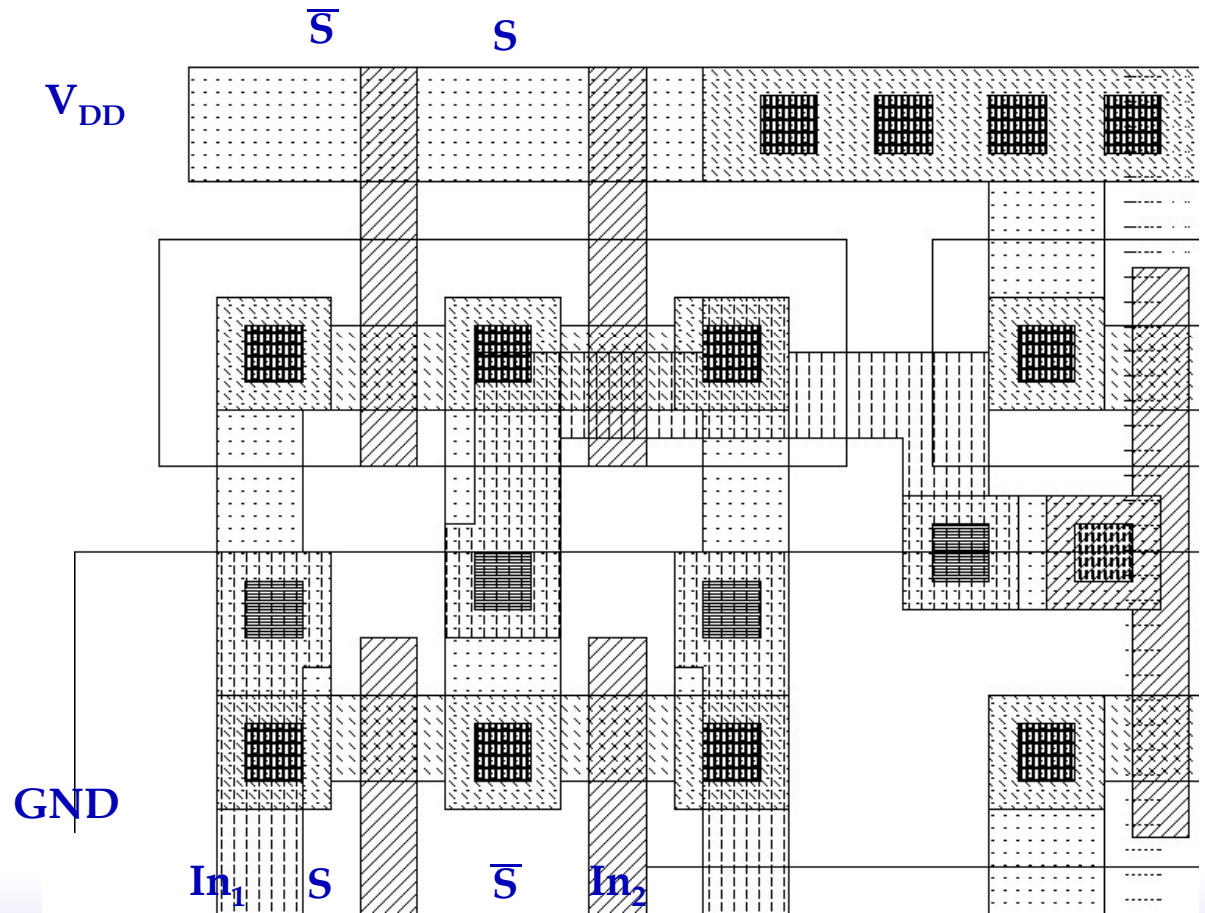
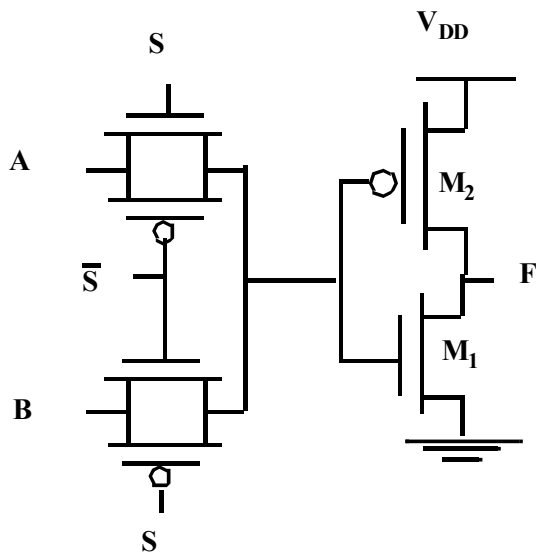
Solution 3: Transmission Gate



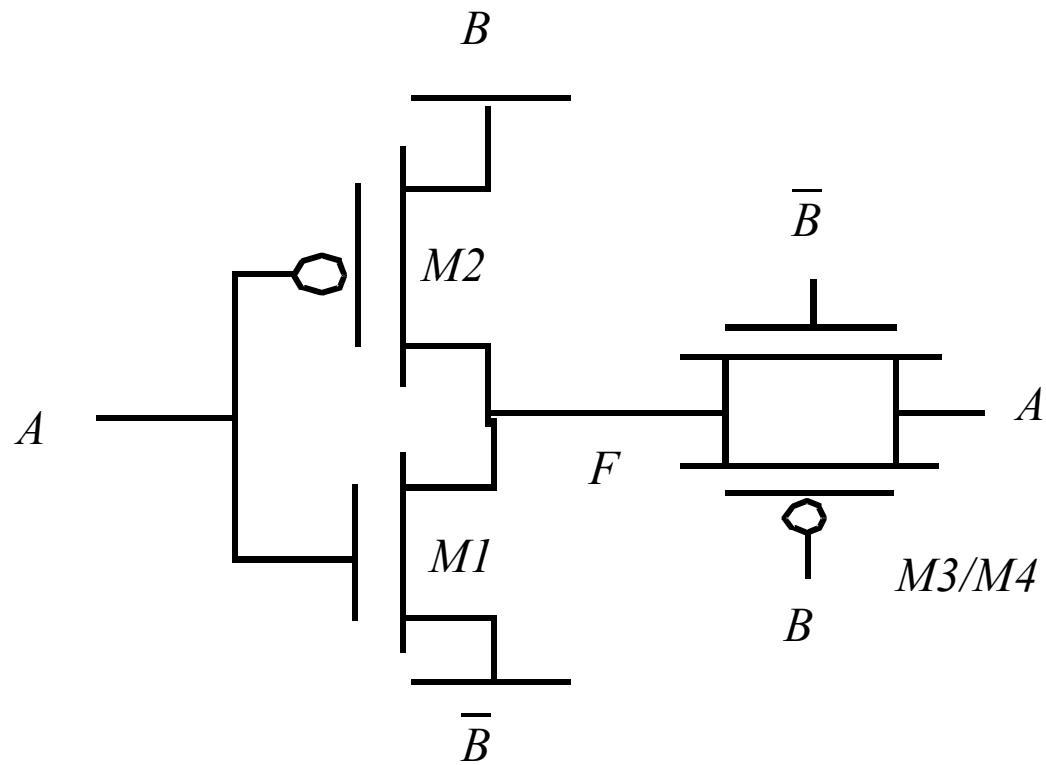
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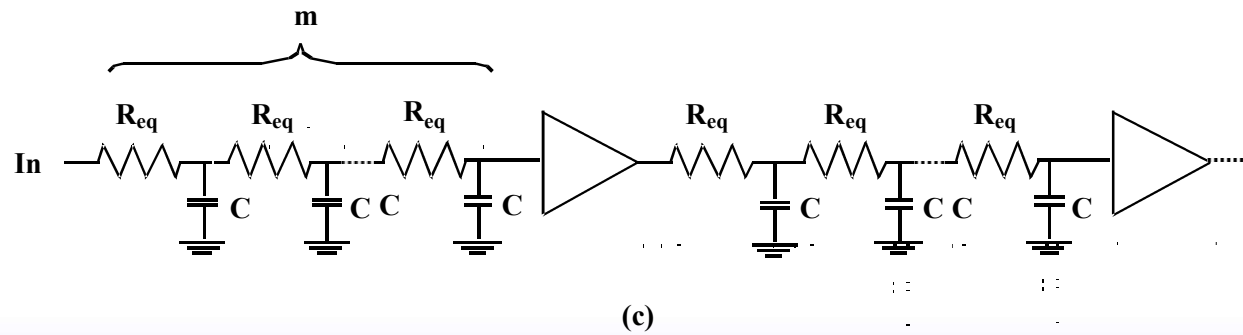
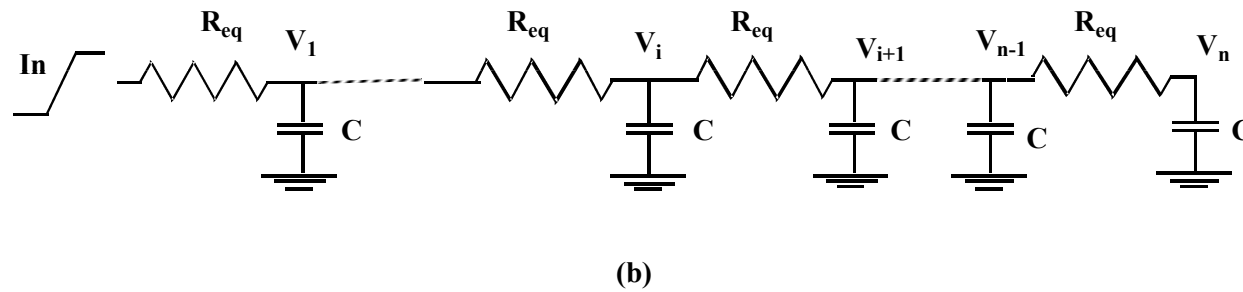
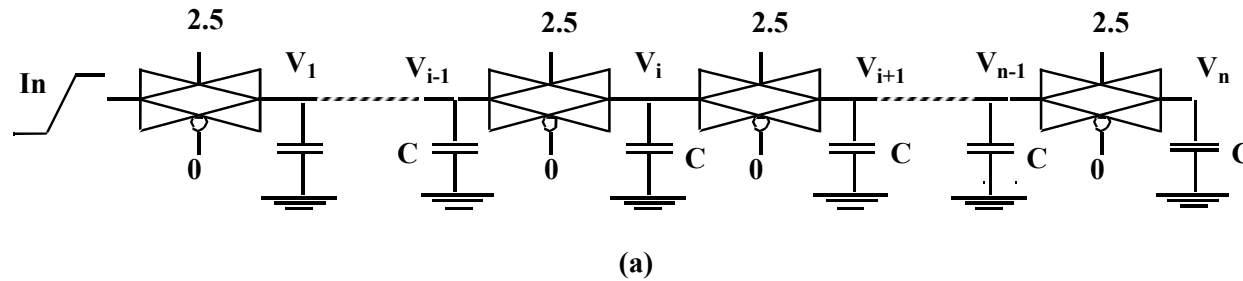
Pass-Transistor Based Multiplexer



Transmission Gate XOR



Delay in Transmission Gate Networks



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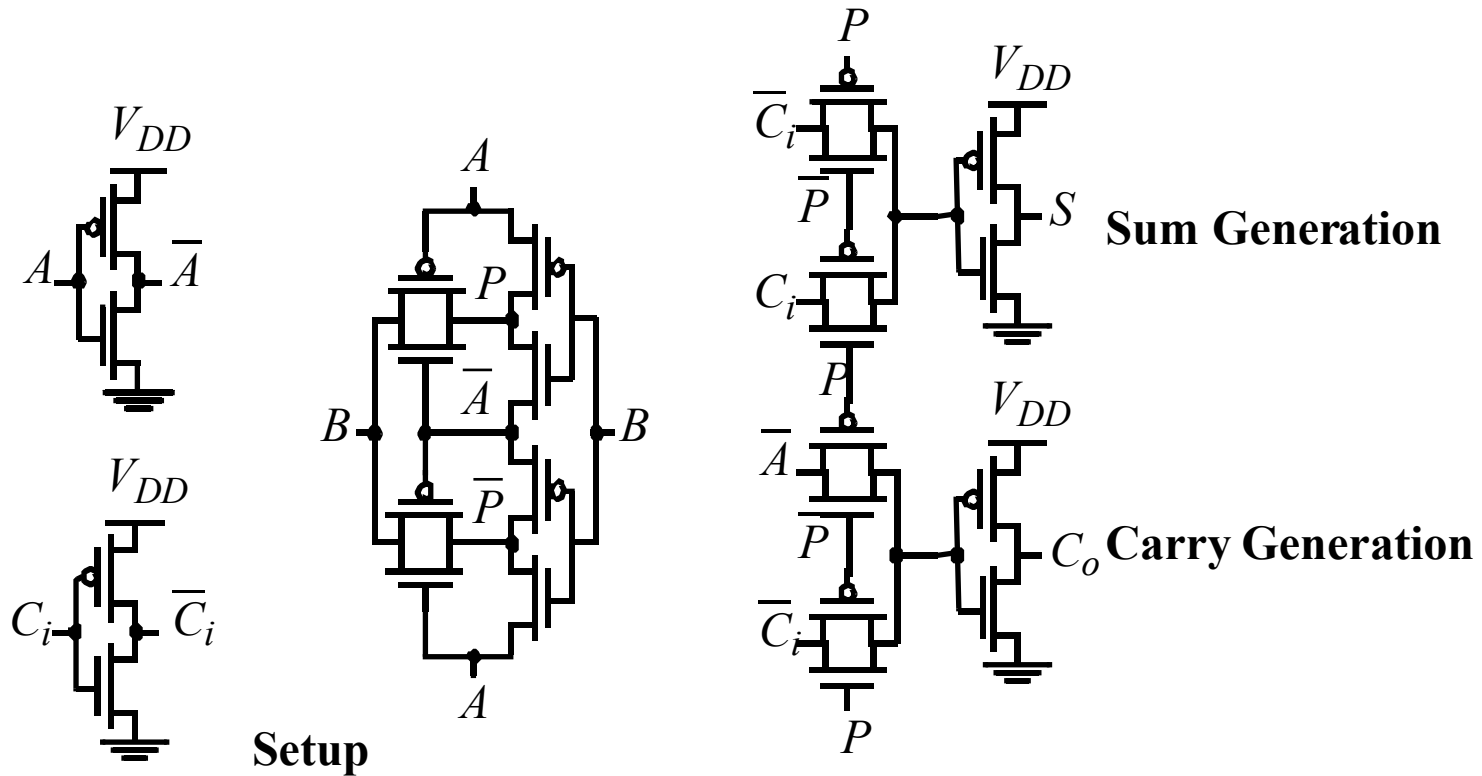
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Transmission Gate Full Adder



Similar delays for sum and carry