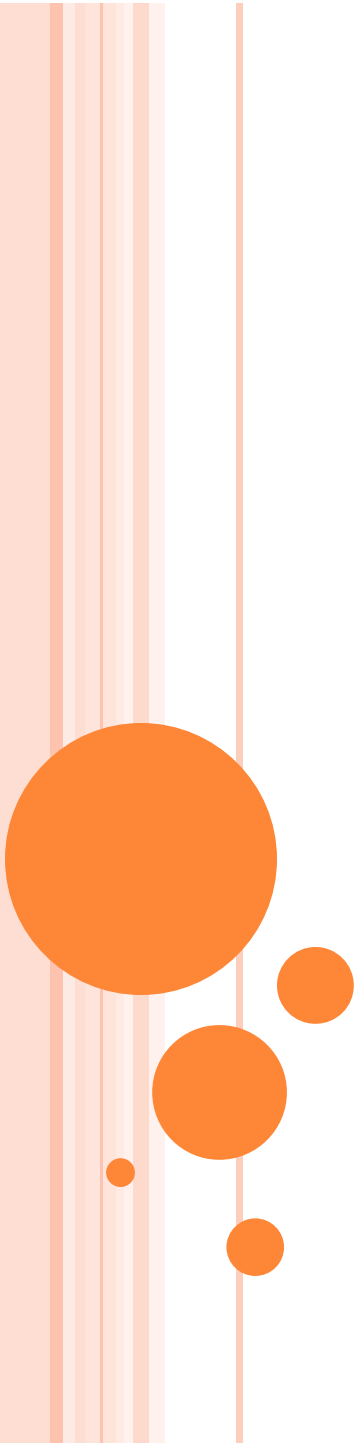


SoC Design Characteristics

SoC Design Characteristics

- Design Level
  - RTL / Behavioral > **Architectural / VC Evaluation**
- Design Team
  - Small, Focused > Multidisciplinary> **Multi-Group, Multidisciplinary**
- Primary Design
  - Custom Logic > Blocks, Custom Interface> **Interface to System / Bus**
- Design Reuse
  - Opportunistic Soft, Firm and Hard > **Planned Firm and Hard**
- Optimization Focus
  - Synthesis, Gate-level > Floor planning, Block Architecture > **System Architecture**

SoC Test Characteristics

- Test Architecture
  - Scan/JTAG/BIST/Custom
    > **Hierarchical**, Parallel scan/JTAG/BIST/custom
- Bus Architecture
  - Custom > **Standardized / Multiple app-specific**
- Verification Level
  - Gate/RTL > Bus functional/RTL/Gate

> **Mixed** (ISS to RTL with H/W and S/W)

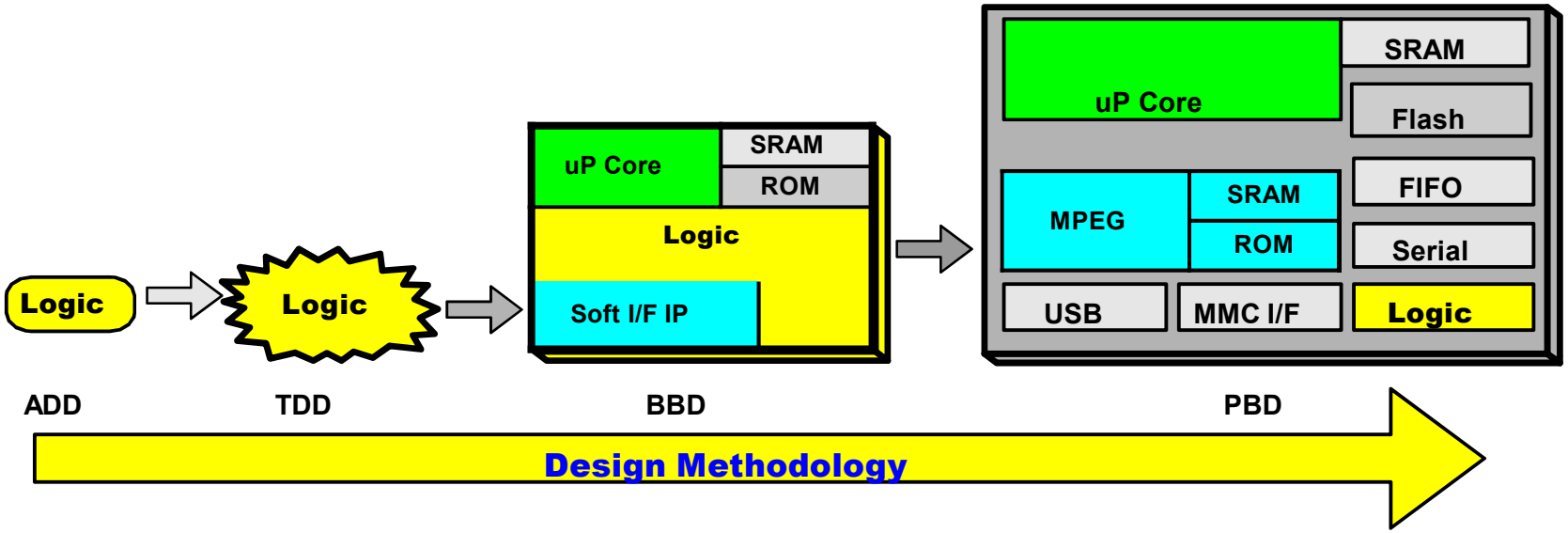
- Partitioning Focus
  - Synthesis limitation > **Functions / Communication**

SoC Layout Characteristics

- Placement
  - Flat > Flat with limited hierarchical > **Hierarchical**
- Routing
  - Flat > Flat with limited hierarchical > **Hierarchical**
- Timing
  - Flat > Flat with limited hierarchical > **Hierarchical**
- Physical Verification
  - Flat > Flat with limited hierarchical > **Hierarchical**

Transition of SoC Design Methodology

- From area-driven to timing-driven design
- From block-based to platform-based design



SoC Design Methodology

- Transition of Design Methodology
  - ADD > TDD > BBD > **PBD**
- Reuse-the key to SoC design
  - Personal > Source > Core > **Virtual Component**
- Integration approach
  - IP-Centric vs. Integration-Centric Approach
- SoC and productivity
  - **Executable specification**
    - Test automation
    - Real-world stimuli
    - Higher-level algorithmic system modeling