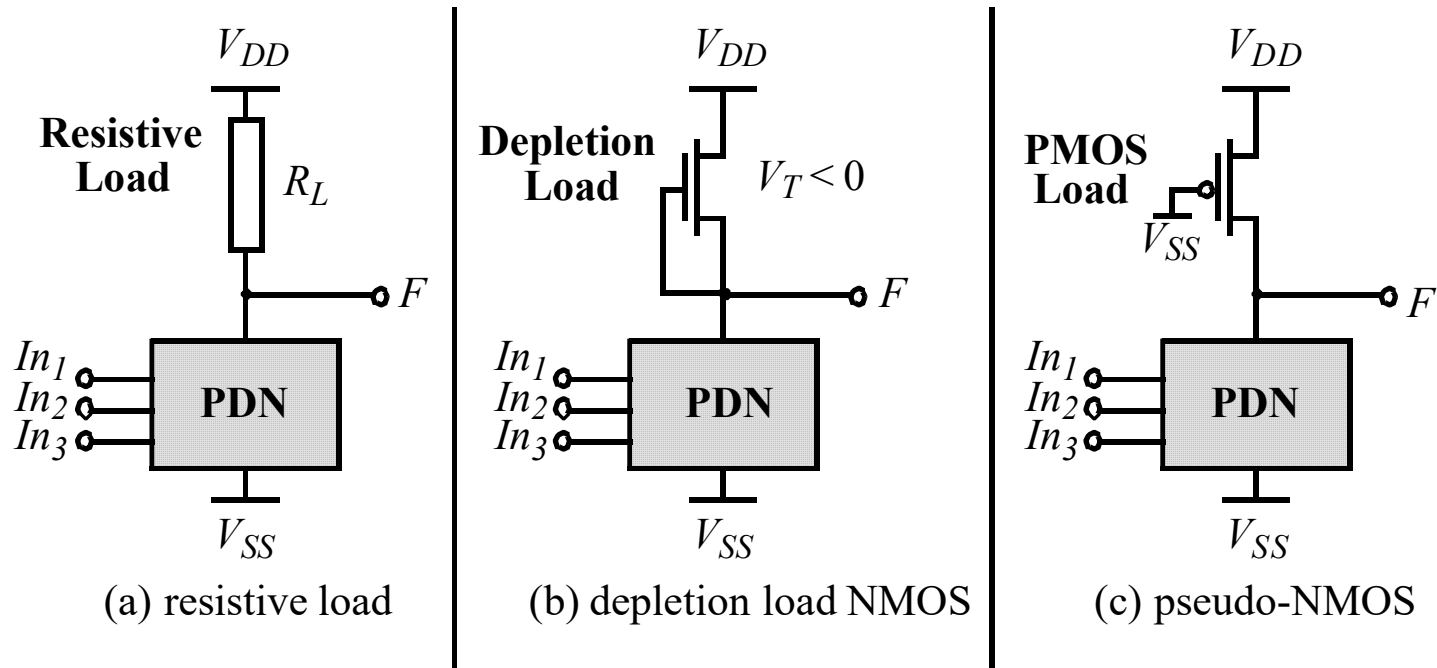


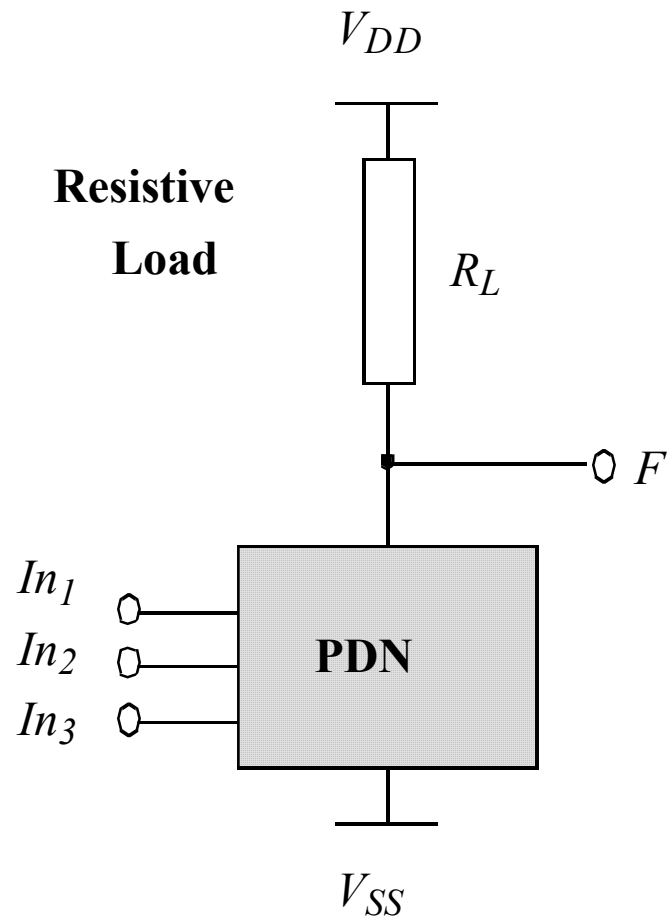
Ratioed Logic

Ratioed Logic



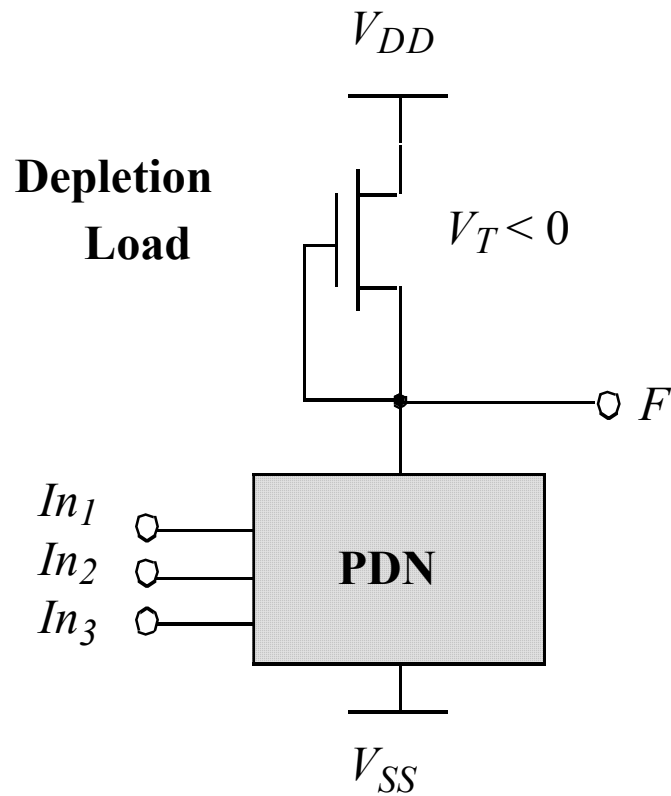
Goal: to reduce the number of devices over complementary CMOS

Ratioed Logic

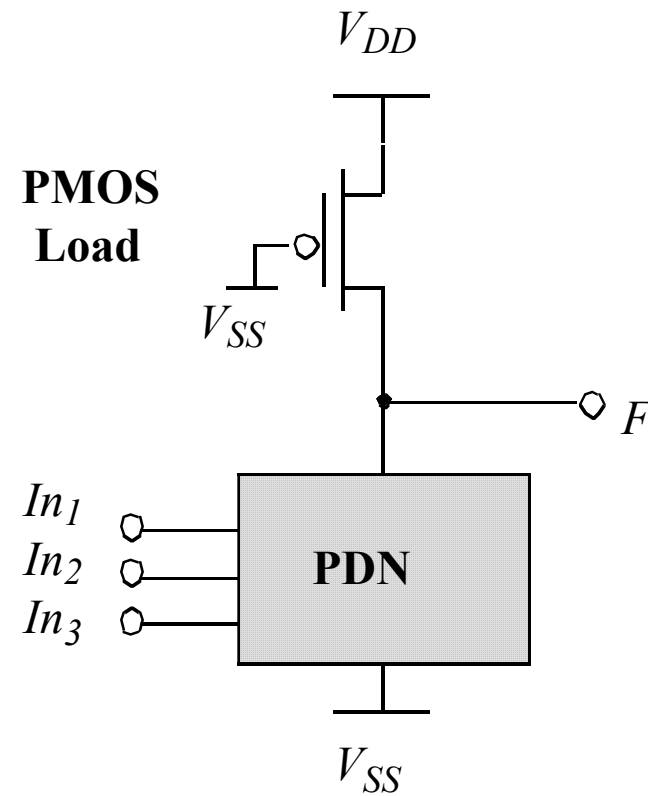


- **N transistors + Load**
- $V_{OH} = V_{DD}$
- $V_{OL} = \frac{R_{PN}}{R_{PN} + R_L}$
- **Assymetrical response**
- **Static power consumption**
- $t_{pL} = 0.69 R_L C_L$

Active Loads

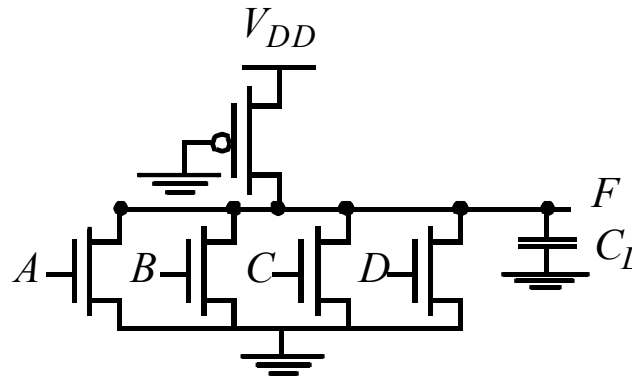


depletion load NMOS



pseudo-NMOS

Pseudo-NMOS



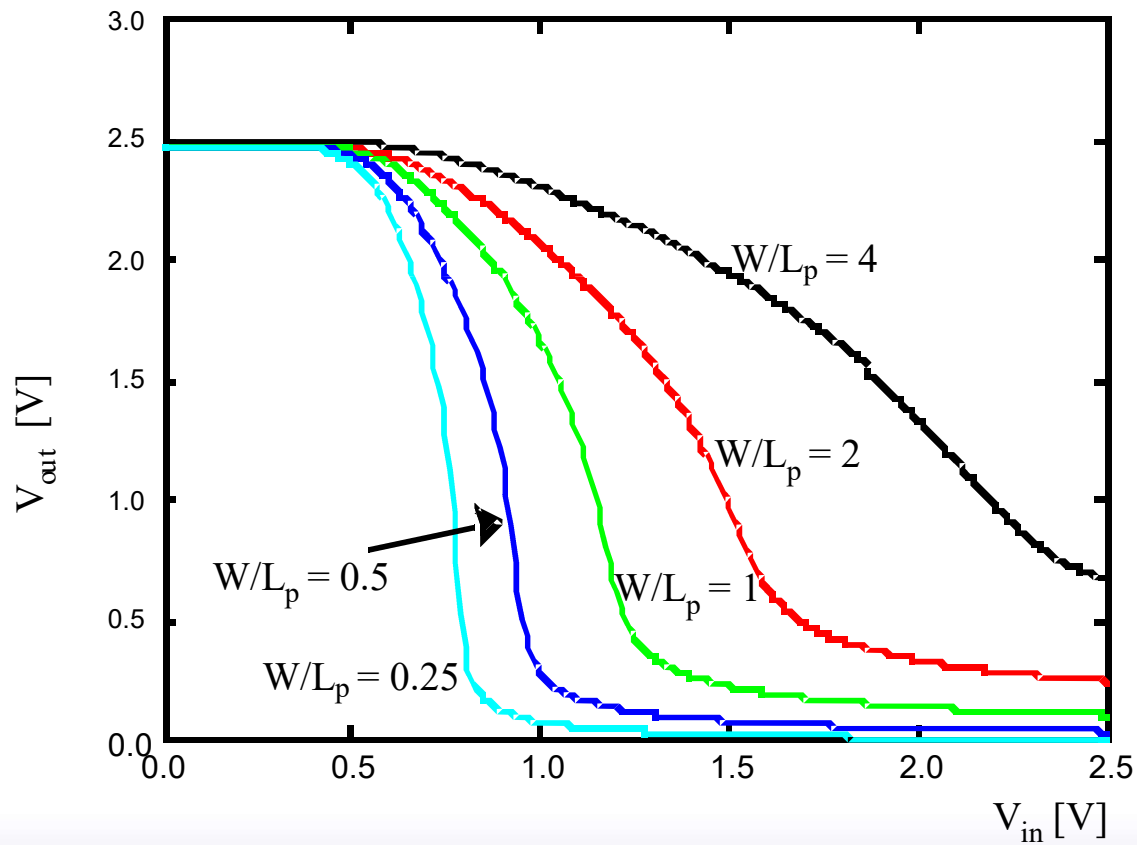
$V_{OH} = V_{DD}$ (similar to complementary CMOS)

$$k_n \left((V_{DD} - V_{Tn}) V_{OL} - \frac{V_{OL}^2}{2} \right) = \frac{k_p}{2} (V_{DD} - |V_{Tp}|)^2$$

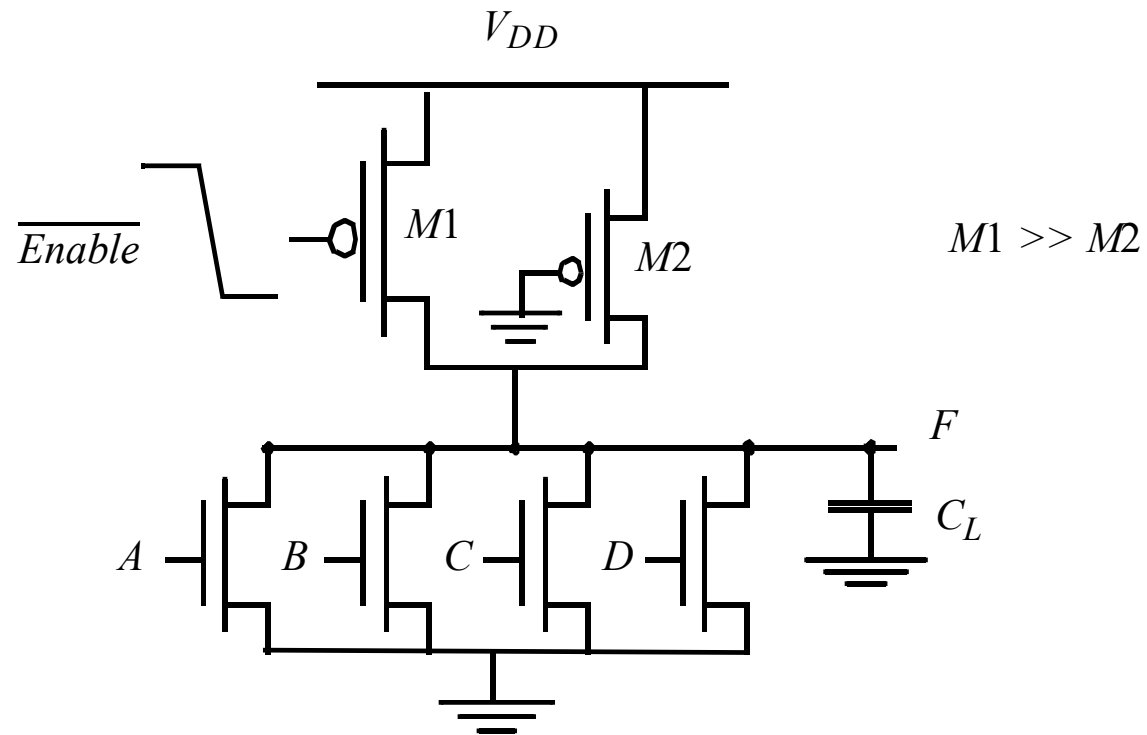
$$V_{OL} = (V_{DD} - V_T) \left[1 - \sqrt{1 - \frac{k_p}{k_n}} \right] \text{ (assuming that } V_T = V_{Tn} = |V_{Tp}| \text{)}$$

SMALLER AREA & LOAD BUT STATIC POWER DISSIPATION!!!

Pseudo-NMOS VTC

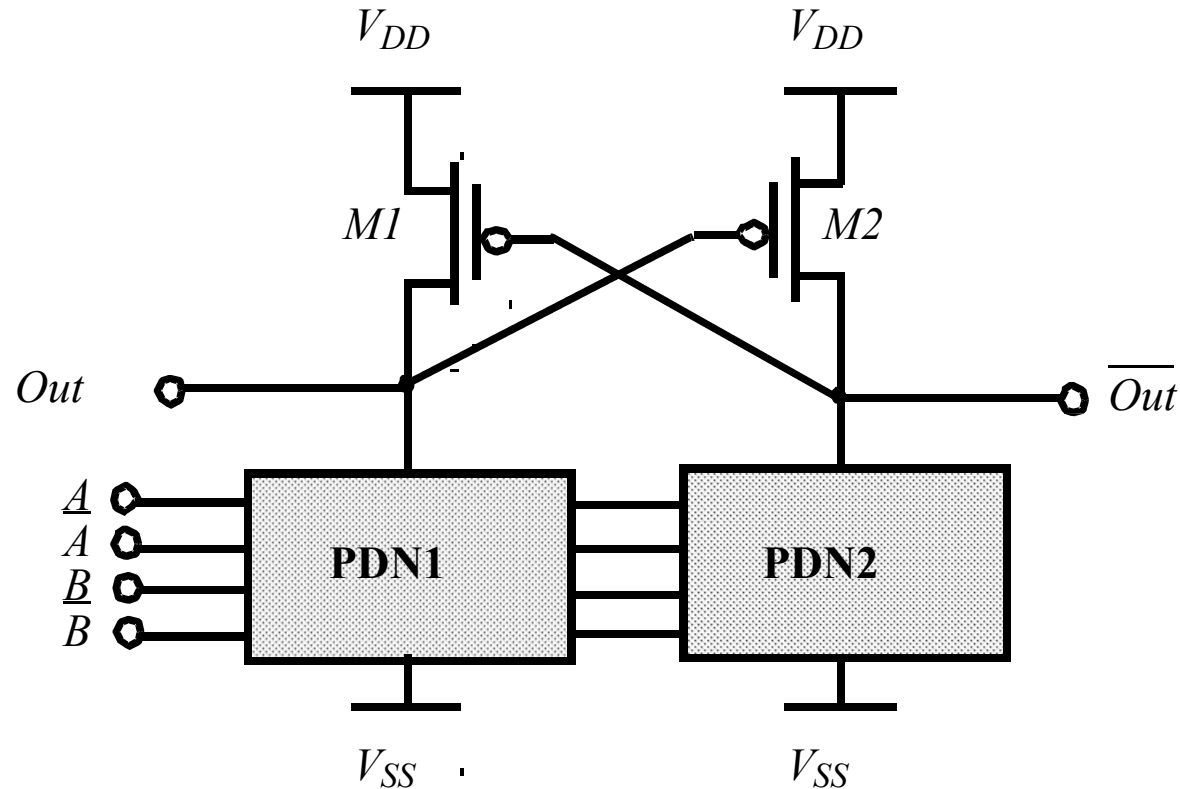


Improved Loads



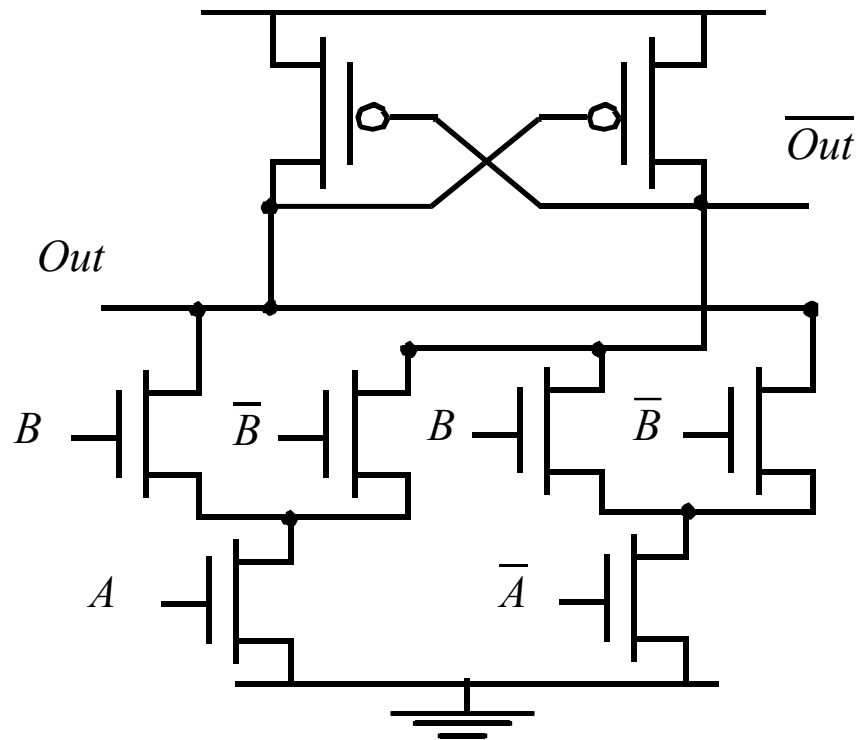
Adaptive Load

Improved Loads (2)



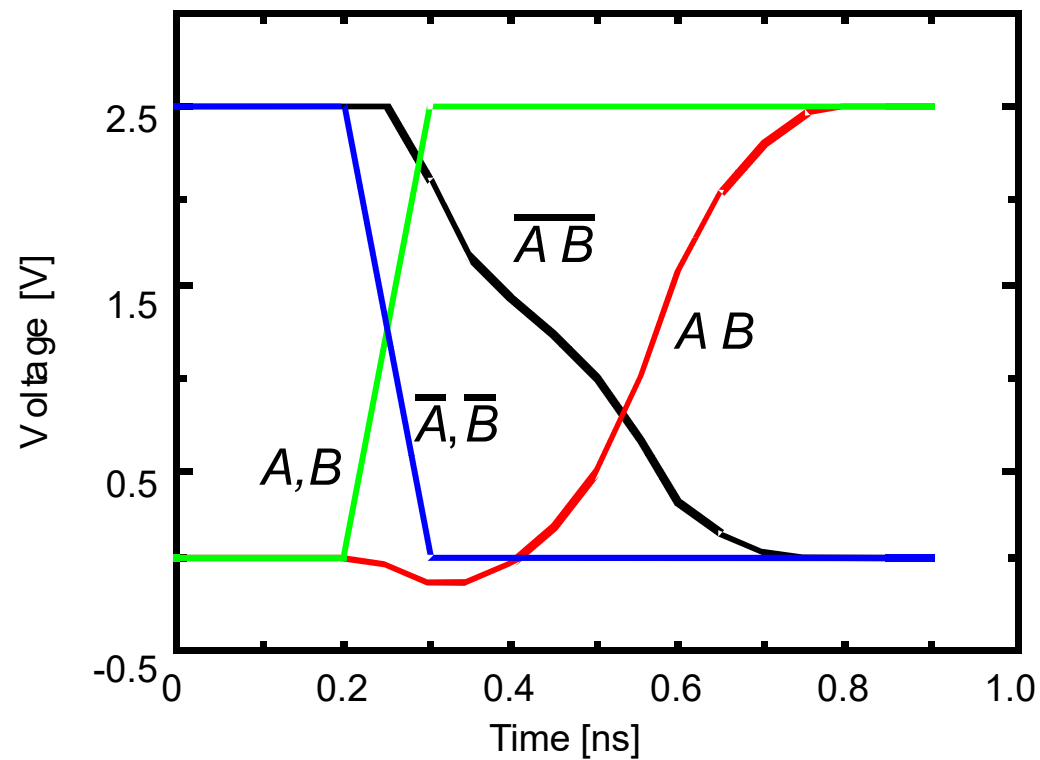
Differential Cascode Voltage Switch Logic (DCVSL)

DCVSL Example



XOR-NXOR gate

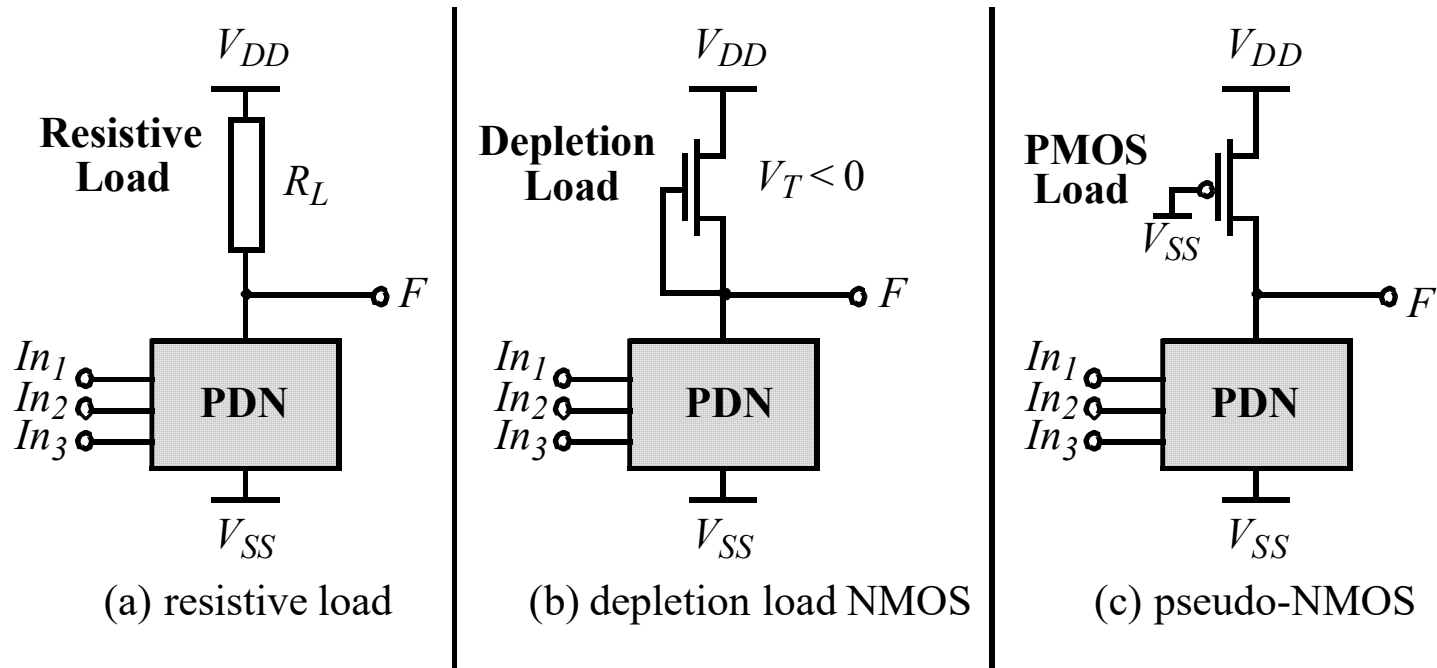
DCVSL Transient Response





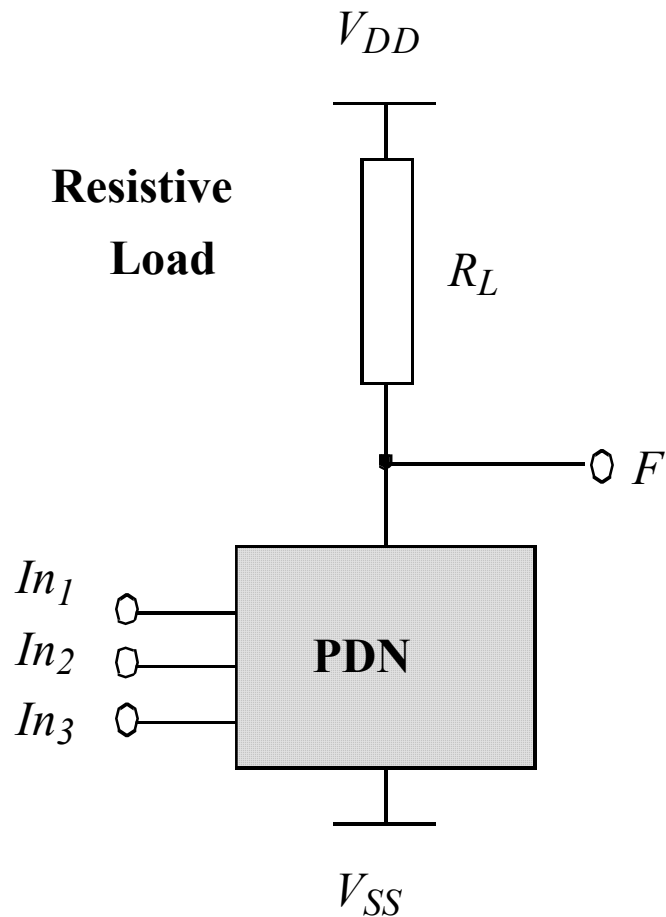
Ratioed Logic

Ratioed Logic



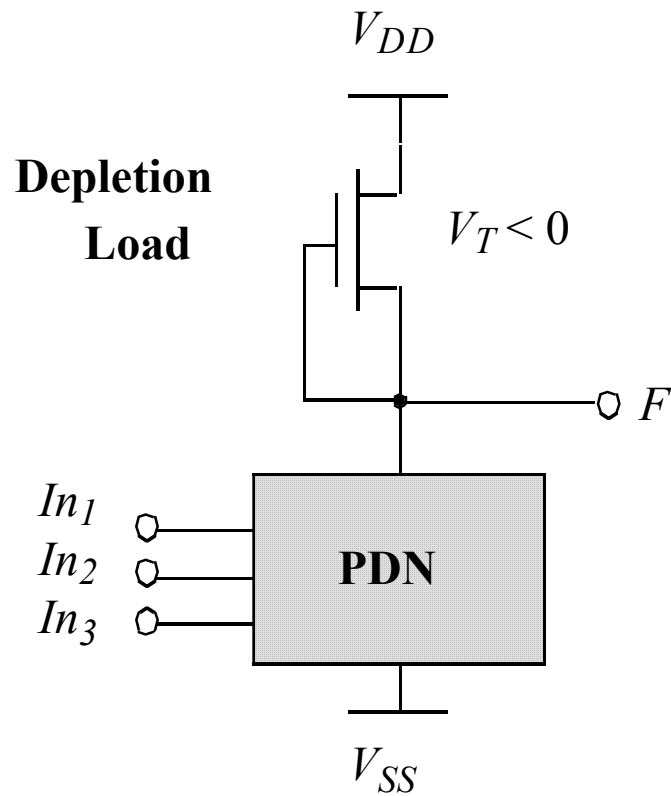
Goal: to reduce the number of devices over complementary CMOS

Ratioed Logic

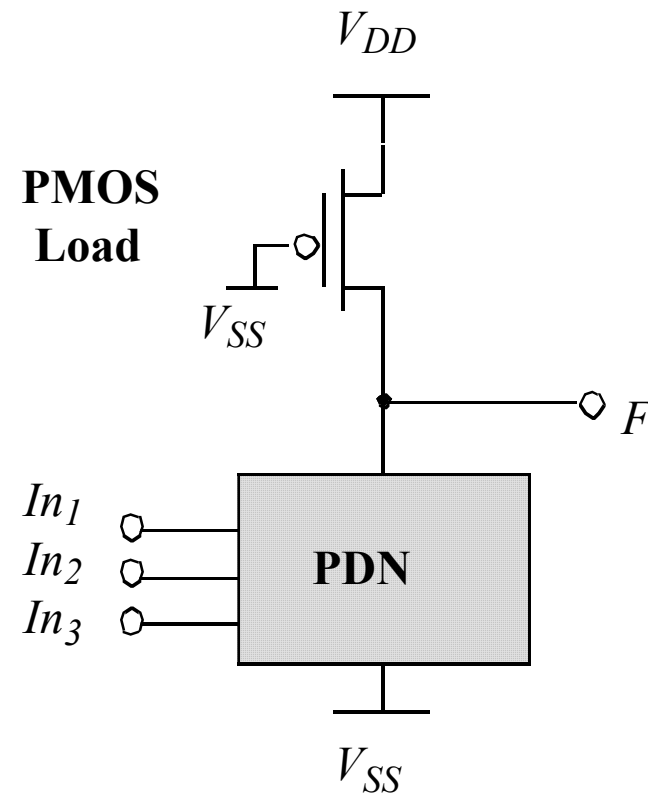


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Active Loads

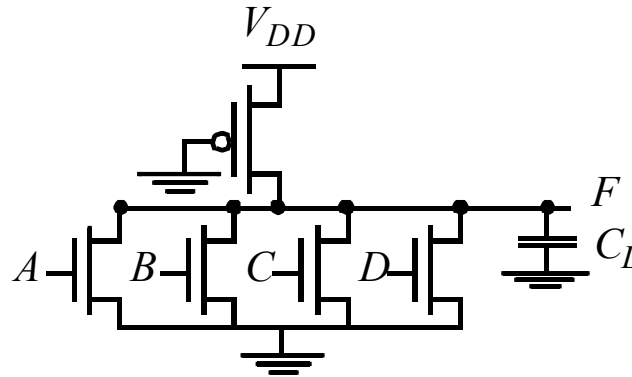


depletion load NMOS



pseudo-NMOS

Pseudo-NMOS



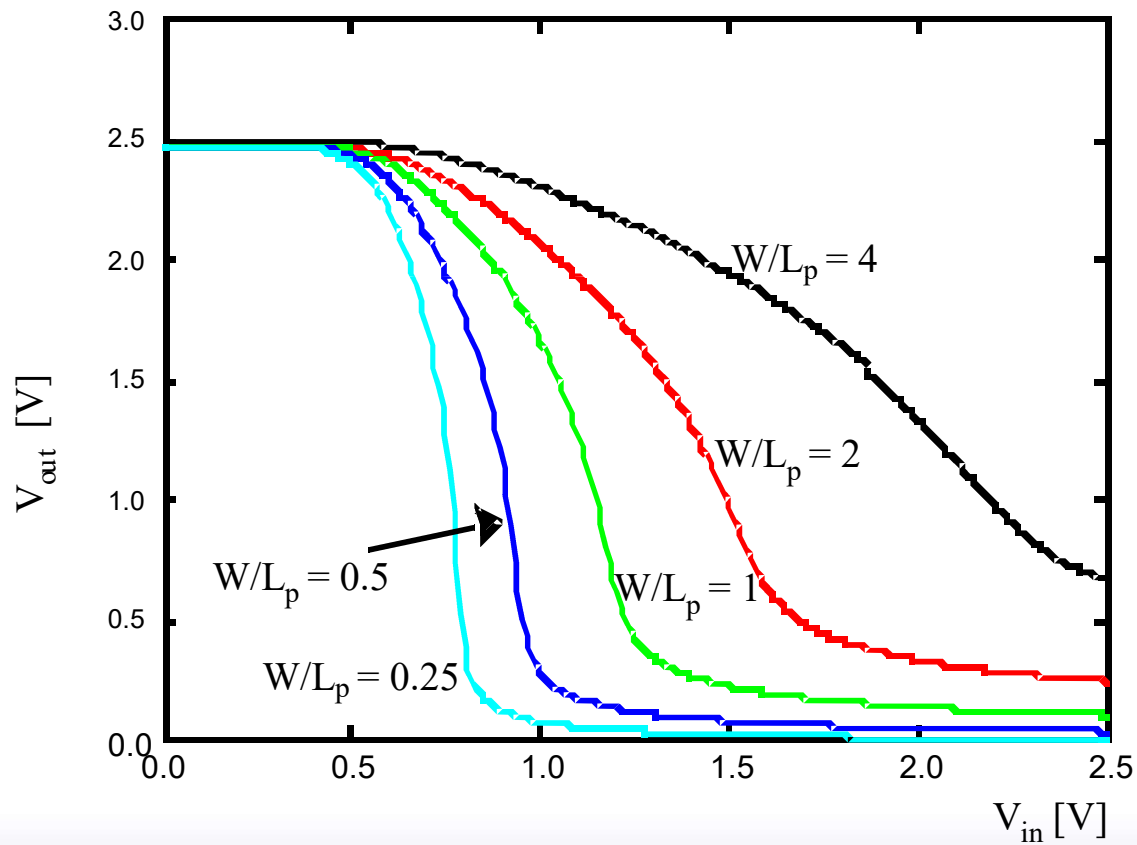
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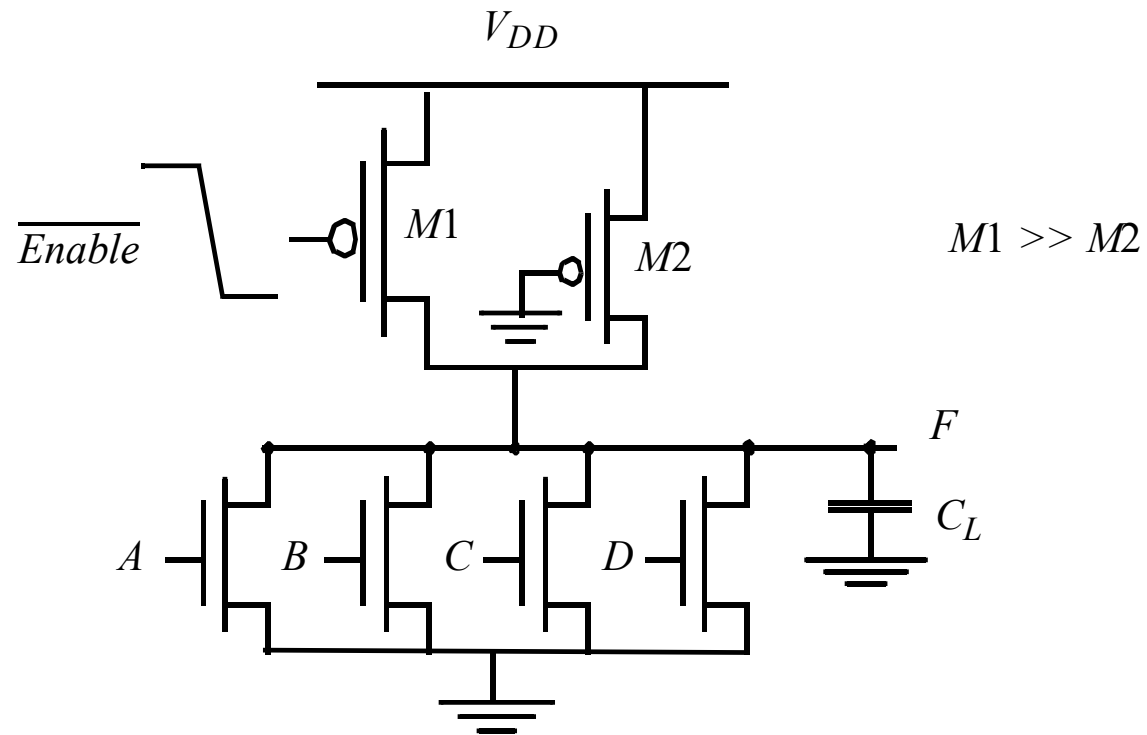
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SMALLER AREA & LOAD BUT STATIC POWER DISSIPATION!!!

Pseudo-NMOS VTC

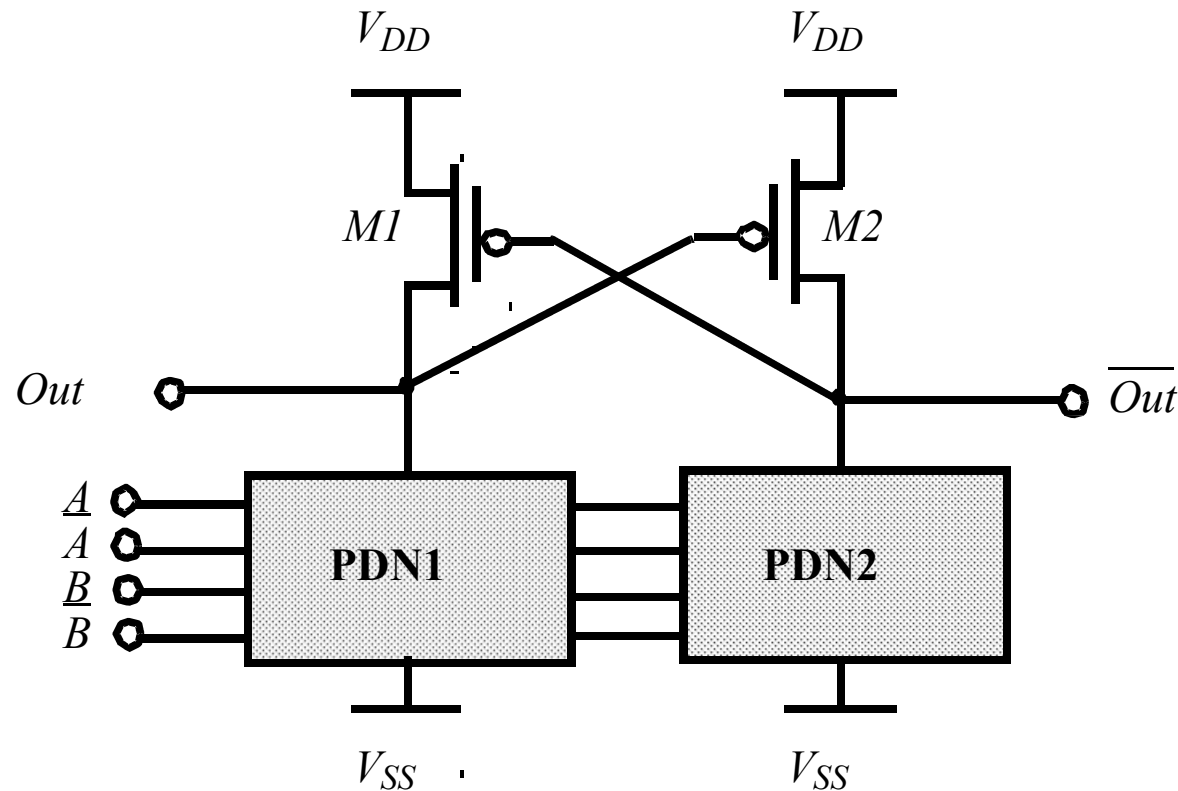


Improved Loads



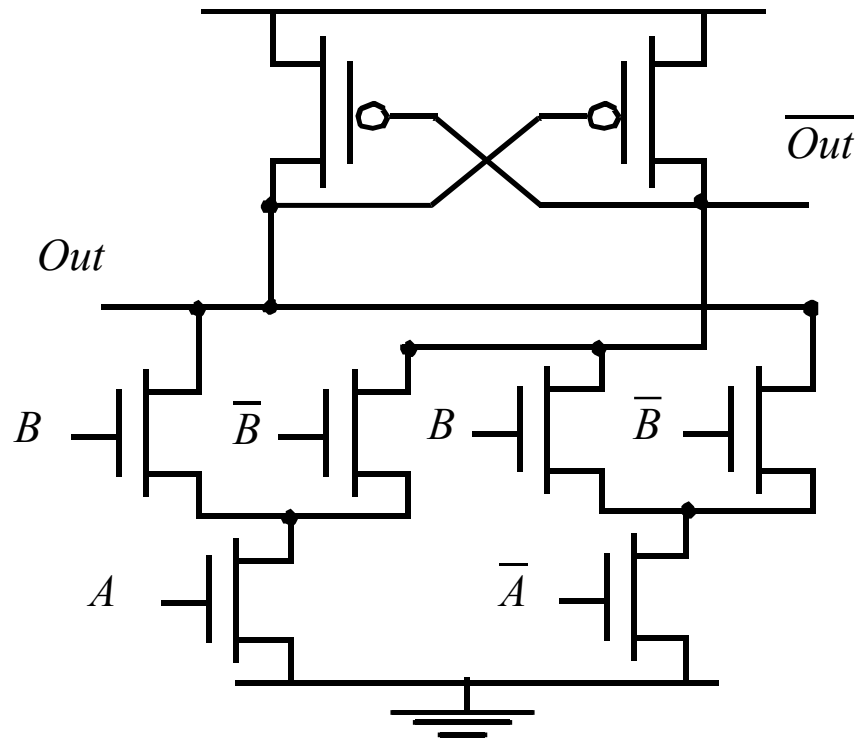
Adaptive Load

Improved Loads (2)



Differential Cascode Voltage Switch Logic (DCVSL)

DCVSL Example



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DCVSL Transient Response

