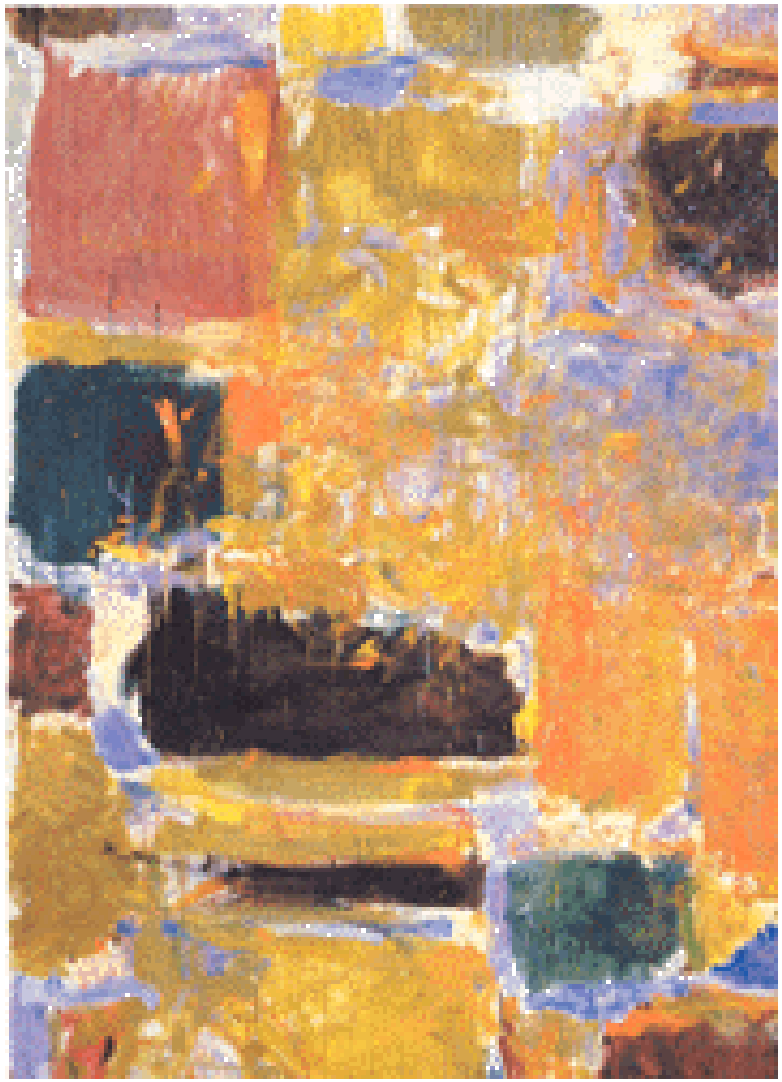


Power Dissipation

Where Does Power Go in CMOS?

- **Dynamic Power Consumption**

  Charging and Discharging Capacitors

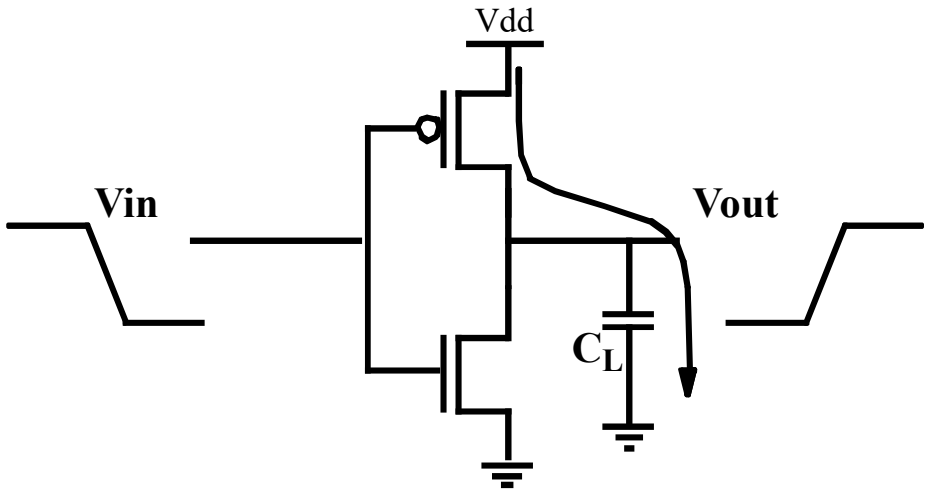
- **Short Circuit Currents**

  Short Circuit Path between Supply Rails during Switching

- **Leakage**

  Leaking diodes and transistors

Dynamic Power Dissipation

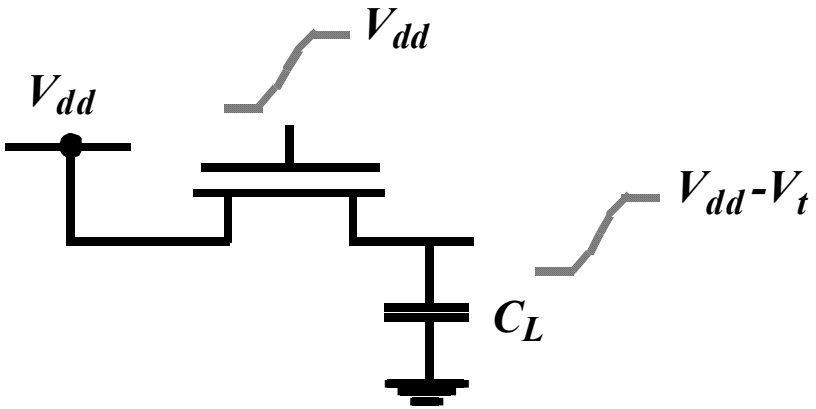


$$\text{Energy/transition} = C_L * V_{dd}^2$$

$$\text{Power} = \text{Energy/transition} * f = C_L * V_{dd}^2 * f$$

- Not a function of transistor sizes!
- Need to reduce C_L, V_{dd}, and f to reduce power.

Modification for Circuits with Reduced Swing

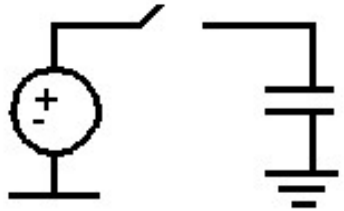


$$E_{0 \rightarrow 1} = C_L \bullet V_{dd} \bullet (V_{dd} - V_t)$$

- **Can exploit reduced swing to lower power (e.g., reduced bit-line swing in memory)**

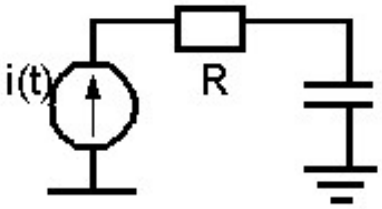
Adiabatic Charging

Charging a capacitor



$CV_{dd}^2/2$

Consider



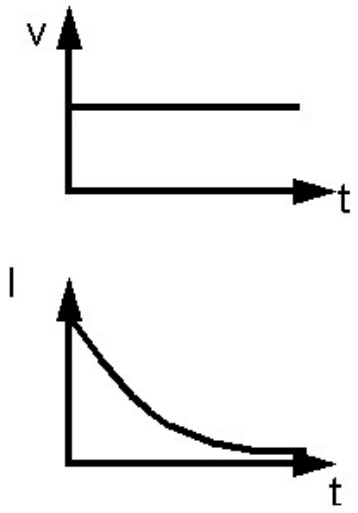
$$v_c = \frac{1}{C}\cdot\int_0^T i\,dt = \frac{1}{C}\cdot I_{av}\cdot T \qquad I_{av} = \frac{C\cdot v_c}{T}$$

$$E_{dis} = R\cdot\int_0^T i^2(t)\,dt \geq R\cdot\int_0^T I_{av}^2\,dt = R\cdot I_{av}^2\cdot T = \frac{RC}{T}\cdot C\cdot V_c^{\,2}$$

Adiabatic Charging

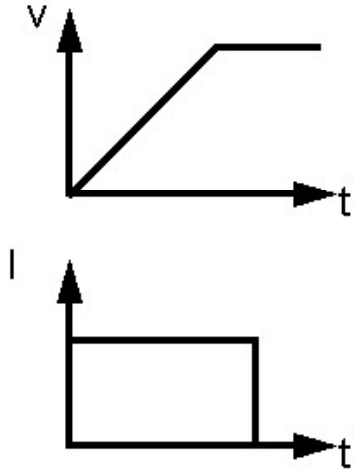
$$V_I = RI + V_c = RC\frac{dv_c}{dt} + V_c$$

V_I = cst -> Exponential current



$E_R = CV_c^2/2$

I = I_{av} -> Linear ramp on V_I



wins if T > 2RC

mimimal energy

$E_R = RC/T\ CV_c^2$

Node Transition Activity and Power

- **Consider switching a CMOS gate for *N* clock cycles**

$$E_N = C_L \bullet V_{dd}^2 \bullet n(N)$$

E_N : the energy consumed for N clock cycles

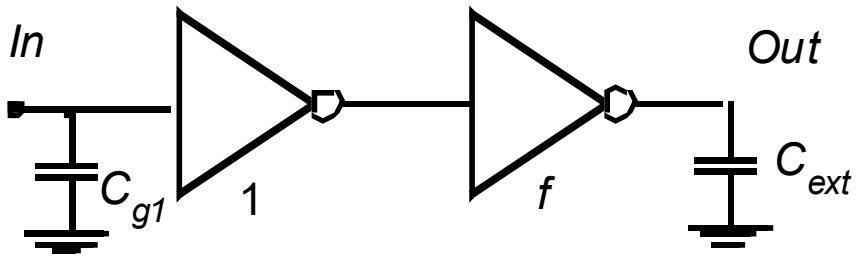
$n(N)$: the number of 0->1 transition in N clock cycles

$$P_{avg} = \lim_{N \to \infty} \frac{E_N}{N} \bullet f_{clk} = \left(\lim_{N \to \infty} \frac{n(N)}{N} \right) \bullet C_L \bullet V_{dd}^2 \bullet f_{clk}$$

$$\alpha_{0 \to 1} = \lim_{N \to \infty} \frac{n(N)}{N}$$

$$\boxed{P_{avg} = \alpha_{0 \to 1} \bullet C_L \bullet V_{dd}^2 \bullet f_{clk}}$$

Transistor Sizing for Minimum Energy



- Goal: Minimize Energy of whole circuit
  - Design parameters: *f* and V_{DD}
  - *tp* ≤ *tpref* of circuit with *f*=1 and $V_{DD} = V_{ref}$

$$t_p = t_{p0}\left(\left(1+\frac{f}{\gamma}\right)+\left(1+\frac{F}{f\gamma}\right)\right)$$

$$t_{p0} \propto \frac{V_{DD}}{V_{DD}-V_{TE}}$$

Transistor Sizing (2)

- Performance Constraint (γ=1)

$$\frac{t_p}{t_{pref}} = \frac{t_{p0}}{t_{p0ref}} \frac{\left(2 + f + \frac{F}{f}\right)}{(3+F)} = \frac{V_{DD}}{V_{ref}} \frac{V_{ref} - V_{TE}}{V_{DD} - V_{TE}} \frac{\left(2 + f + \frac{F}{f}\right)}{(3+F)} = 1$$

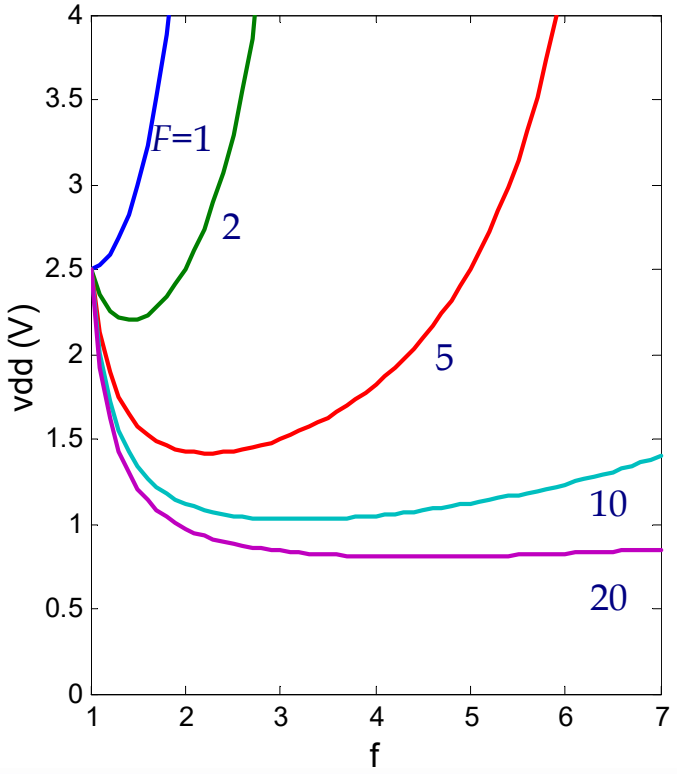
- Energy for single Transition

$$E = V_{DD}^2 C_{g1} \left[(1+\gamma)(1+f) + F\right]$$

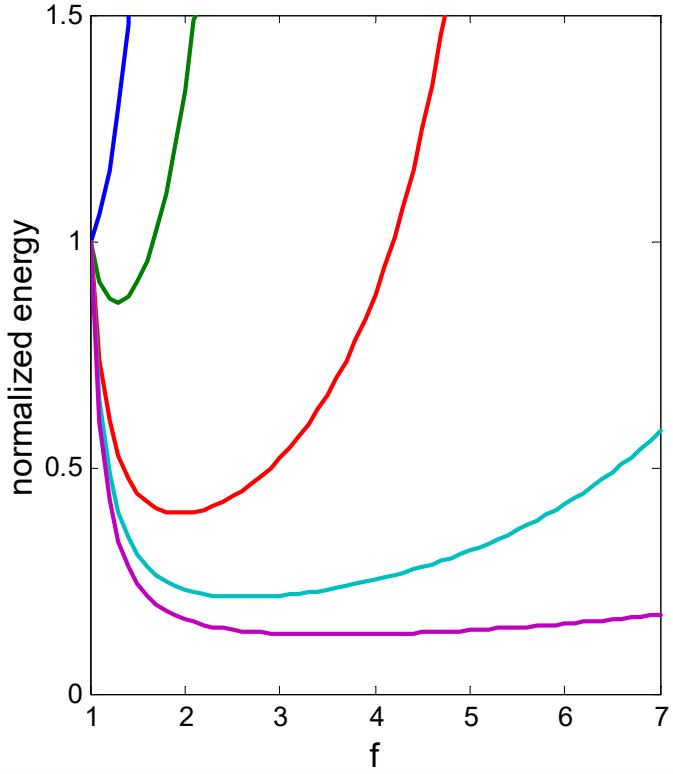
$$\frac{E}{E_{ref}} = \left(\frac{V_{DD}}{V_{ref}}\right)^2 \left(\frac{2 + 2f + F}{4 + F}\right)$$

Transistor Sizing (3)

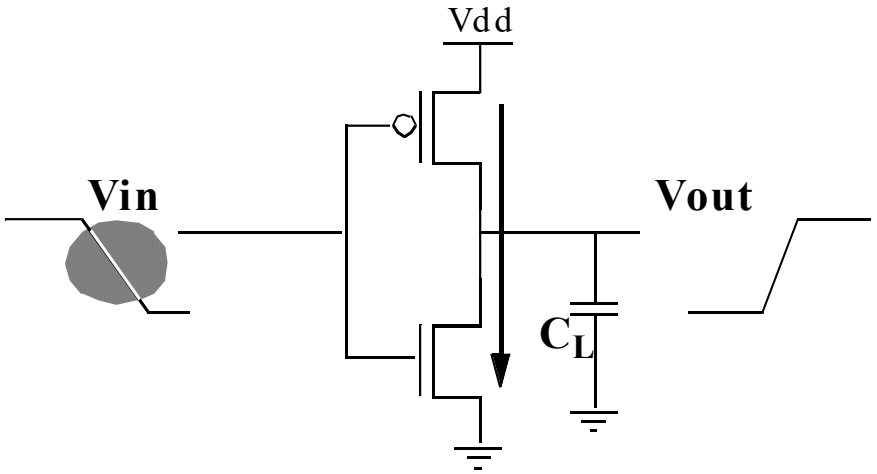
V_{DD}=f(f)

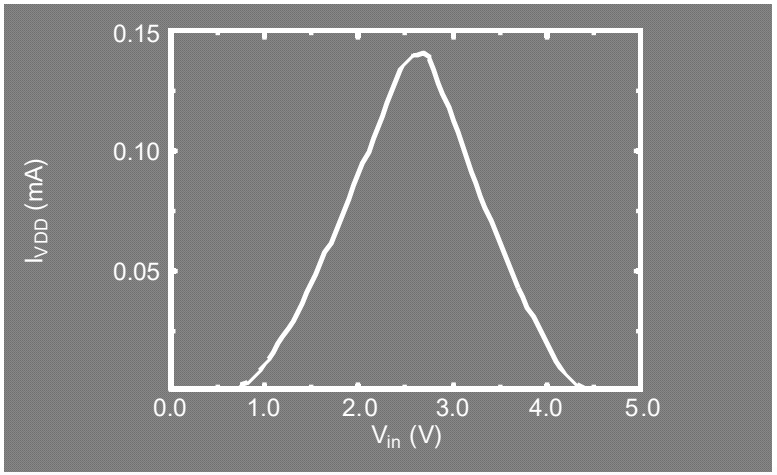


E/E_{ref}=f(f)

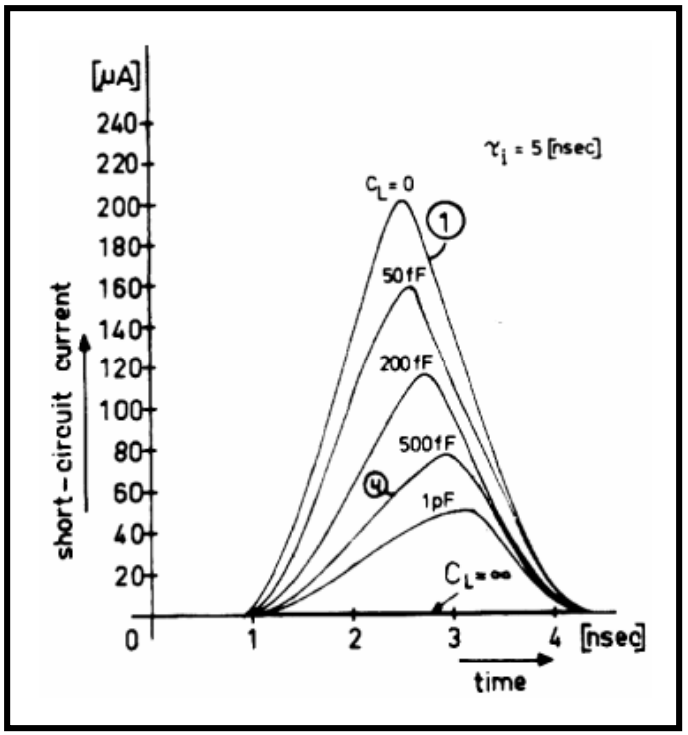


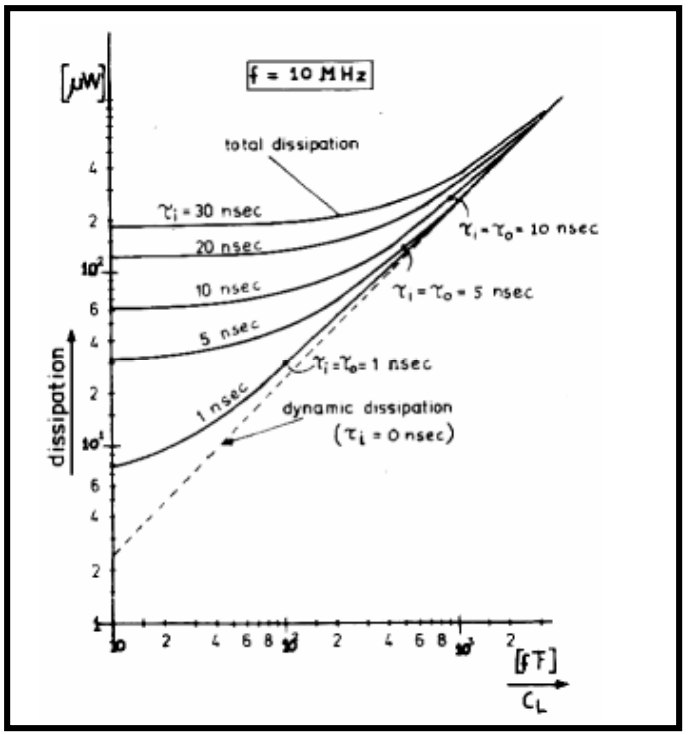
Short Circuit Currents





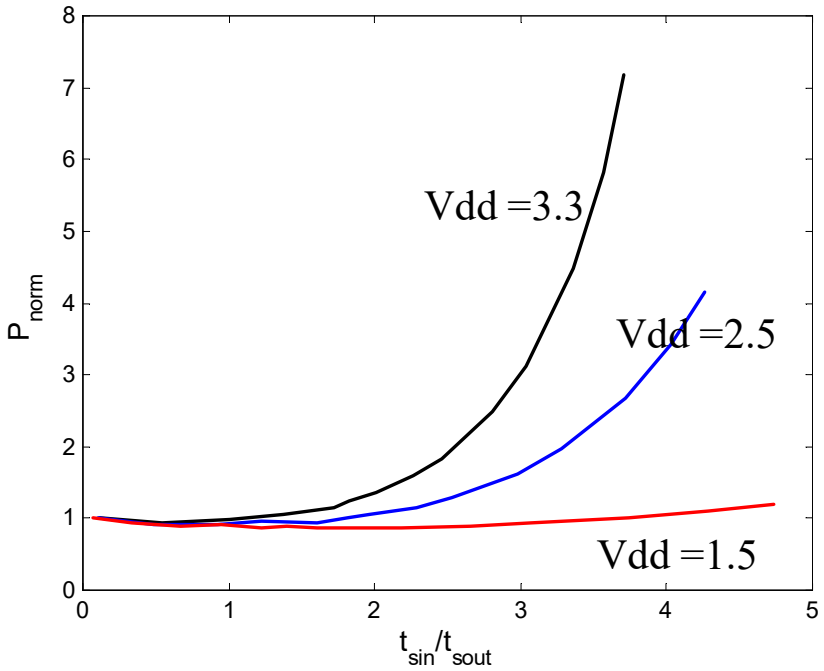
How to keep Short-Circuit Currents Low?





Short circuit current goes to zero if $t_{fall} >> t_{rise}$,
but can't do this for cascade logic, so ...

Minimizing Short-Circuit Power



- Keep the input and output rise/fall times the same (< 10% of Total Consumption)

from [Veendrick84]

(*IEEE Journal of Solid-State Circuits*, August 1984)

- If $V_{dd} < V_{tn} + |V_{tp}|$ then short-circuit power can be *eliminated*!