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FSM and Efficient Synthesizable FSM Design using Verilog



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Introduction

There are many ways to code FSMs including many very poor ways to code FSMs.

This lecture offers guidelines for doing efficient coding, simulation and synthesis of FSM designs.

In this lecture multiple references are made to combinational always blocks and sequential always blocks.



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Introduction

Combinational *always* blocks are *always* blocks that are used to code combinational logic functionality and are strictly coded using *blocking assignments*. A combinational always block has a combinational sensitivity list, a sensitivity list without "*posedge*" or "*negedge*" Verilog keywords.

Sequential *always* blocks are *always* blocks that are used to code clocked or sequential logic and are always coded using *nonblocking* assignments. A sequential always block has an edge-based sensitivity list.



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Mealy & Moore FSMs

A common classification used to describe the type of an FSM is Mealy and Moore state machines.

A Moore FSM is a state machine where the outputs are only a function of the present state.

A Mealy FSM is a state machine where one or more of the outputs is a function of the present state and one or more of the inputs.

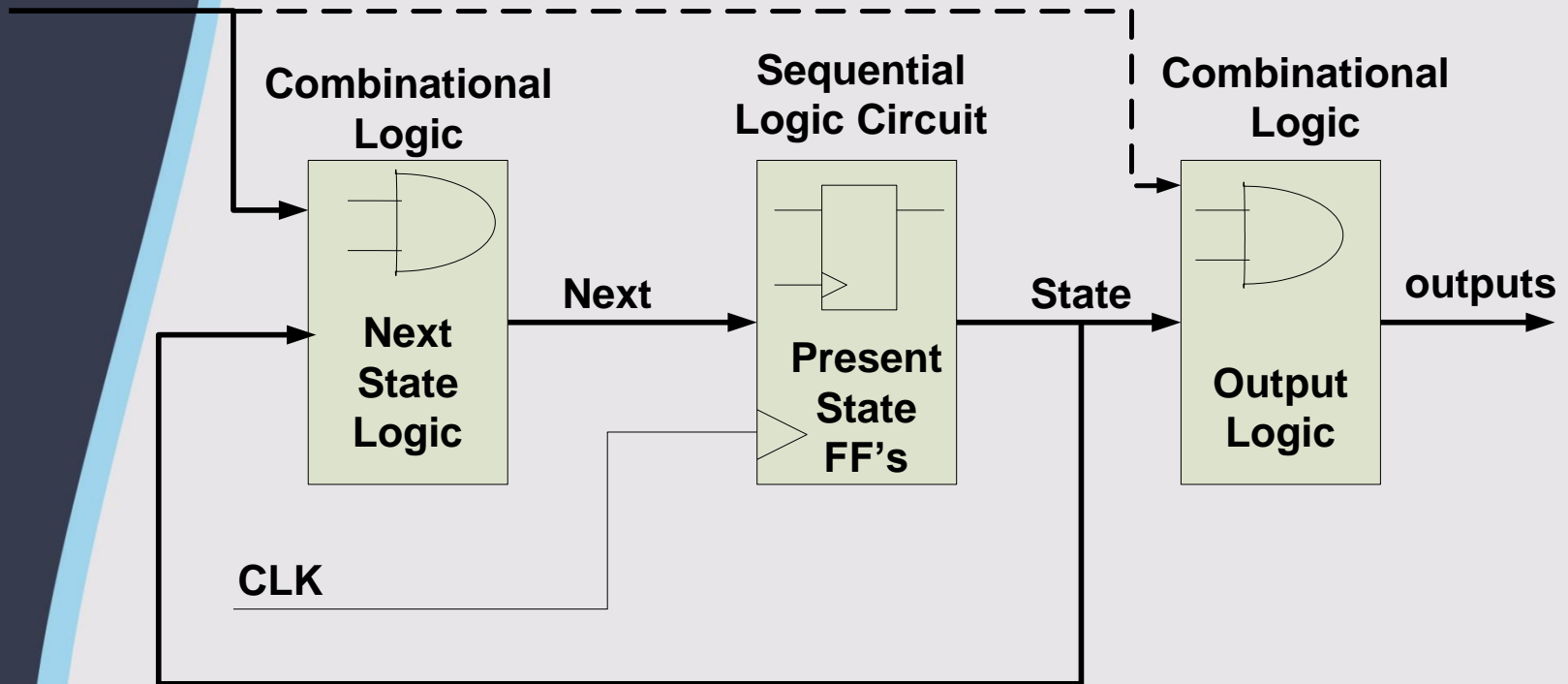


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Mealy & Moore FSMs (contd.)

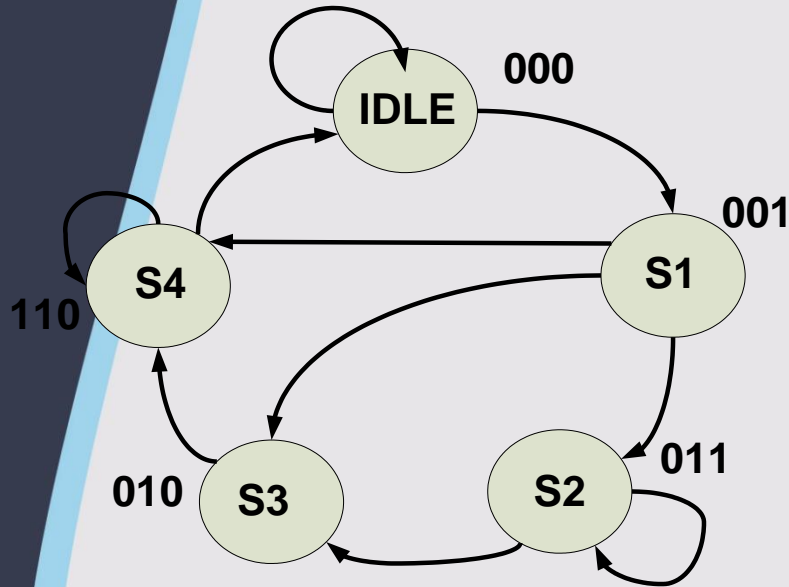
Mealy Machine Only



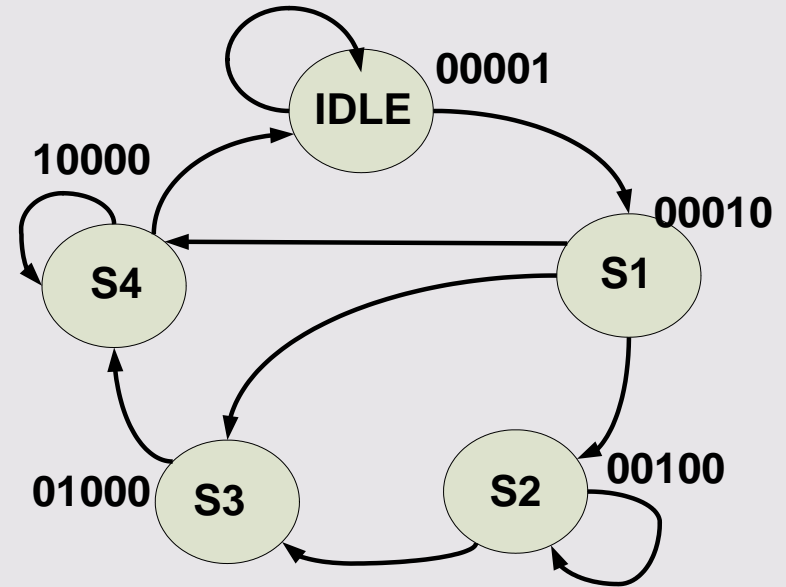


Binary Encoded or One Hot Encoding

**Binary Encoded FSM
(Highly Encoded)**



One Hot Encoding





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Binary Encoded or One Hot Encoding

A binary-encoded FSM design only requires as many flip-flops as are needed to uniquely encode the number of states in the state machine.

Number of FF

if($\log_2(\text{number of states}) == \text{integer}$)

required FF = $\log_2(\text{number of states})$

else

required FF = $\text{integer}(\log_2(\#\text{states})) + 1$;



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Binary Encoded or One Hot Encoding

A onehot FSM design requires a flip-flop for each state in the design and only one flip-flop (the flip-flop representing the current or "hot" state) is set at a time in a onehot FSM design.

For a state machine with 9-16 states, a binary FSM only requires 4 flip-flops while a onehot FSM requires a flip-flop for each state in the design (9-16 flip-flops).



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FSM Coding Goals

What constitutes an efficient FSM coding style?

Identify HDL coding goals and why they are important.

Quantify the capabilities of various FSM coding styles.



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FSM Coding Goals

- The FSM coding style should be easily modified to change state encodings and FSM styles.
- The coding style should be compact.
- The coding style should be easy to code and understand.
- The coding style should facilitate debugging.
- The coding style should yield efficient synthesis results.