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Introduction to ASICs

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ASICs

ASIC - Application Specific Integrated Circuit
- In Integrated Circuit (IC) designed to perform a specific function for a specific application
- As opposed to a standard, general purpose off-the-shelf part such as a commercial microprocessor or a 7400 series IC

Gate equivalent - a unit of size measurement corresponding to a 4 transistor gate equivalent (e.g. a 2 input NOR gate)

Levels of integration:
- SSI - Small scale integration
- MSI - Medium scale integration
- LSI - Large scale integration
- VLSI - Very large scale integration
- USLI - Ultra large scale integration

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An Integrated Circuit

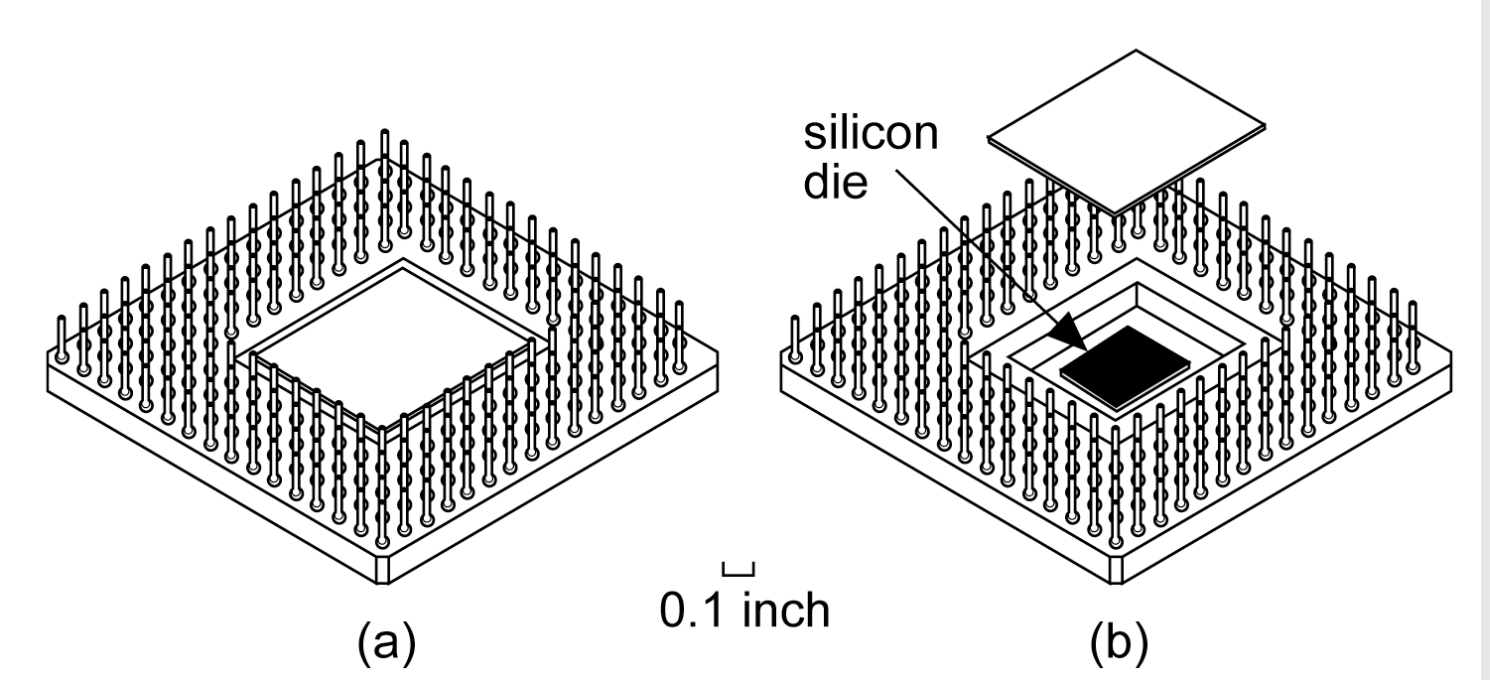

Figure 1.1 A packaged Integrated Circuit (IC)

Types of ASICs

Full-Custom ASICs

Standard-Cell–Based ASICs

Gate-Array–Based ASICs

Channeled Gate Array

Channelless Gate Array

Structured Gate Array

Programmable Logic Devices

Field-Programmable Gate Arrays

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Full-Custom ASICs

- All mask layers are customized in a full-custom ASIC
  - Generally, the designer lays out all cells by hand
  - Some automatic placement and routing may be done
  - Critical (timing) paths are usually laid out completely by hand
- Full-custom design offers the highest performance and lowest part cost (smallest die size) for a given design
- The disadvantages of full-custom design include increased design time, complexity, design expense, and highest risk
- Microprocessors (strategic silicon) were exclusively full-custom, but designers are increasingly turning to semicustom ASIC techniques in this area as well

Standard-Cell-Based ASICs

A cell-based ASIC (CBIC —“sea-bick”)

Standard cells

Possibly megacells , megafunctions , full-custom blocks , system-level macros(SLMs), fixed blocks , cores , or Functional Standard Blocks (FSBs)

All mask layers are customized - transistors and interconnect

- Automated buffer sizing, placement and routing

Custom blocks can be embedded

Manufacturing lead time is about eight weeks.

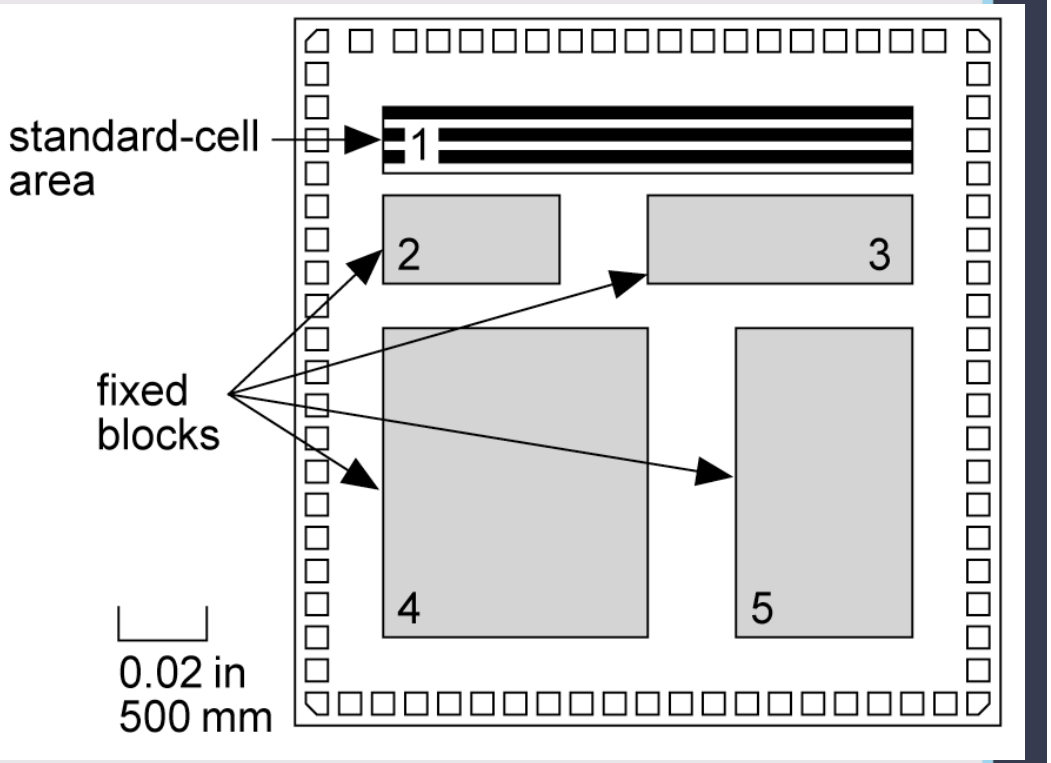

Figure 1.2 A cell-based ASIC (CBIC)

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Standard Cell Layout

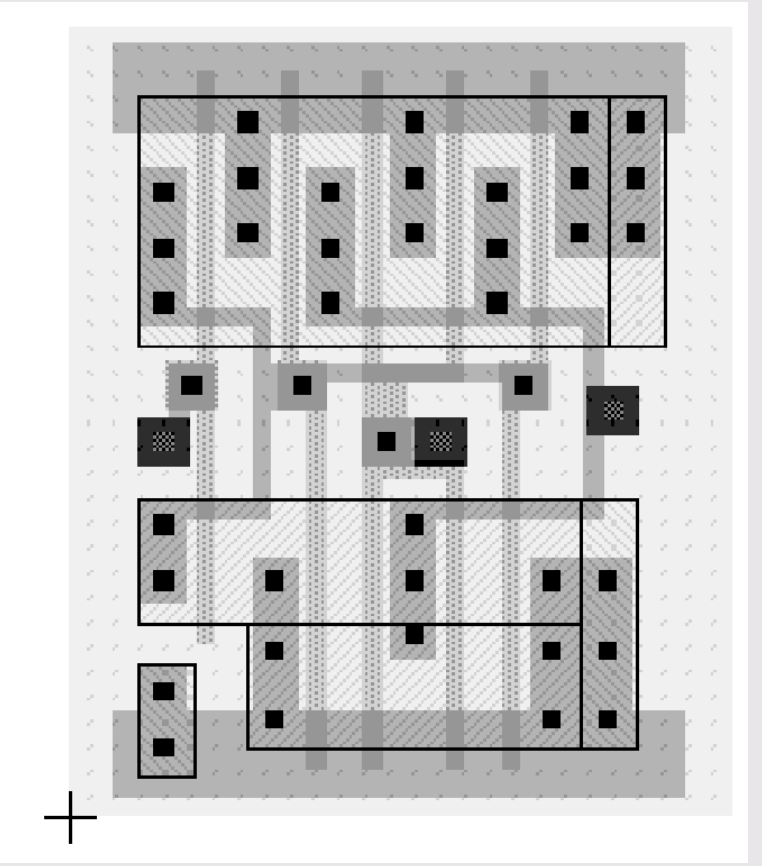

Figure 1.3 Layout of a standard cell

Standard Cell ASIC Routing

- A "wall" of standard cells forms a flexible block
- Metal2 may be used in a feedthrough cell to cross over cell rows that use metal1 for wiring
- Other wiring cells: spacer cells , row-end cells , and power cells

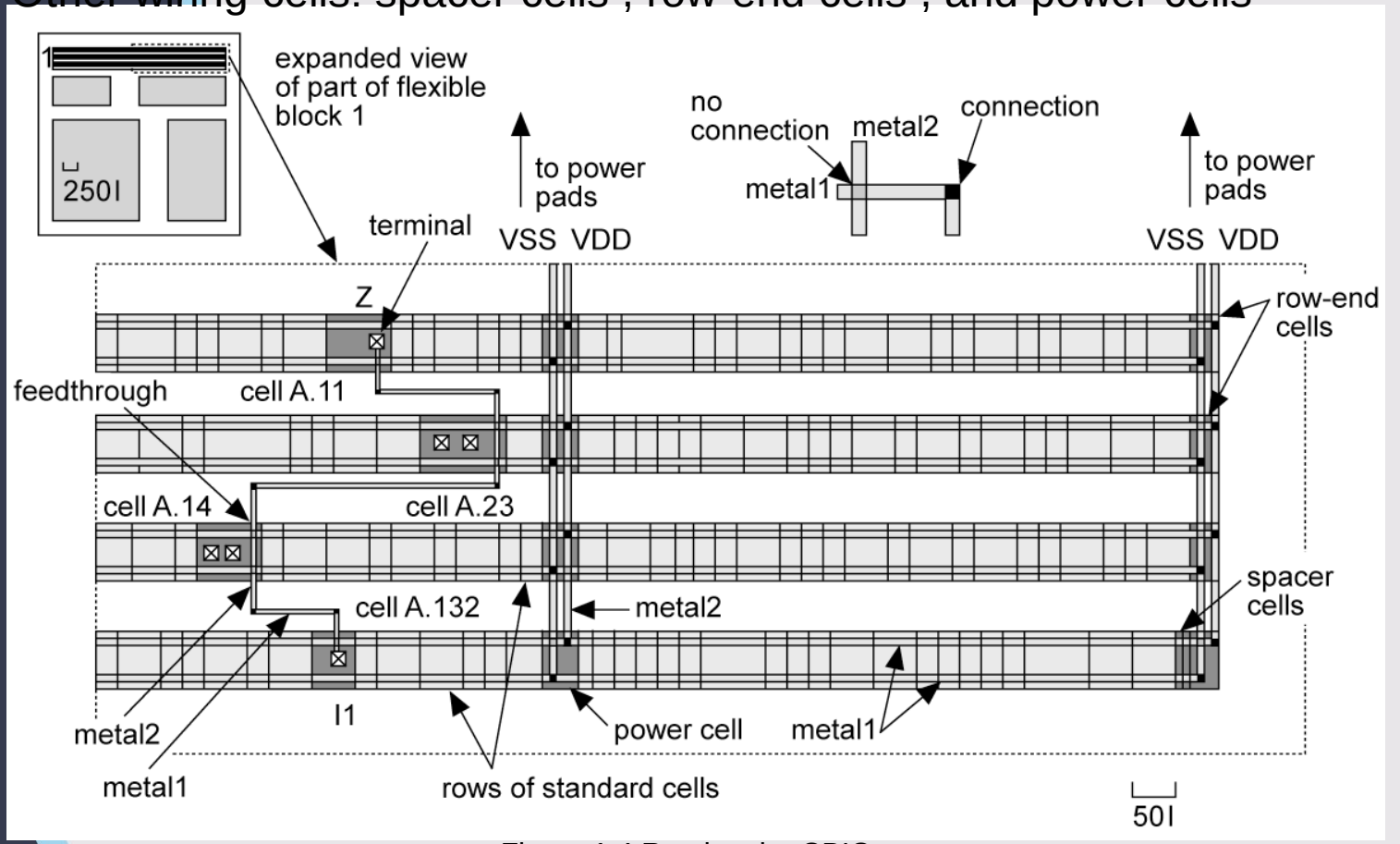

Figure 1.4 Routing the CBIC

Gate-Array-Based ASICs

- In a gate-array-based ASIC, the transistors are predefined on the silicon wafer
- The predefined pattern of transistors is called the *base array*
- The smallest element that is replicated to make the base array is called the *base* or *primitive cell*
- The top level interconnect between the transistors is defined by the designer in custom masks - *Masked Gate Array (MGA)*
- Design is performed by connecting predesigned and characterized logic cells from a library (macros)
- After validation, automatic placement and routing are

Gate-Array-Based ASICs

- Channeled Gate Array
  - Only the interconnect is customized
  - The interconnect uses predefined spaces between rows of base cells
  - Manufacturing lead time is between two days and two weeks

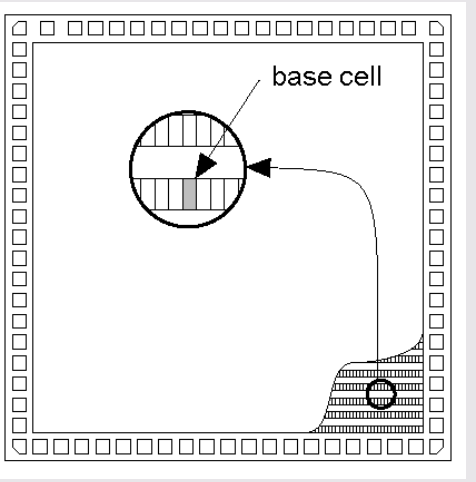

Figure 1.5 Channel gate-array die

- Channelless Gate Array
  - There are no predefined areas set aside for routing - routing is over the top of the gate-array devices
  - Achievable logic density is higher than for channeled gate arrays
  - Manufacturing lead time is between two days and two weeks

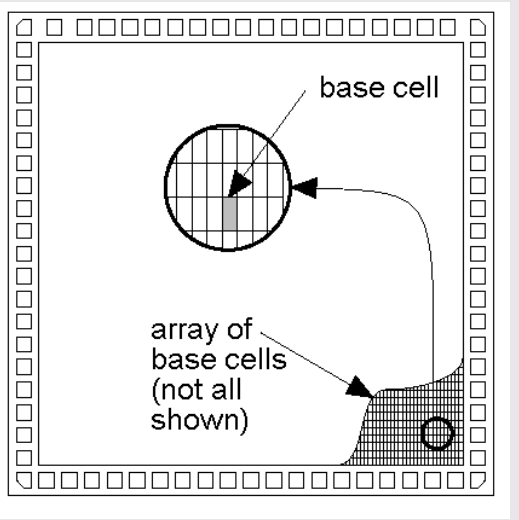

Figure 1.6 Sea-Of-Gates (SOG) array die

Gate-Array-Based ASICs (cont.)

- Structured Gate Array
  - Only the interconnect is customized
  - Custom blocks (the same for each design) can be embedded
    - These can be complete blocks such as a processor or memory array, or
    - An array of different base cells better suited to implementing a specific function
  - Manufacturing lead time is between two days and two weeks.

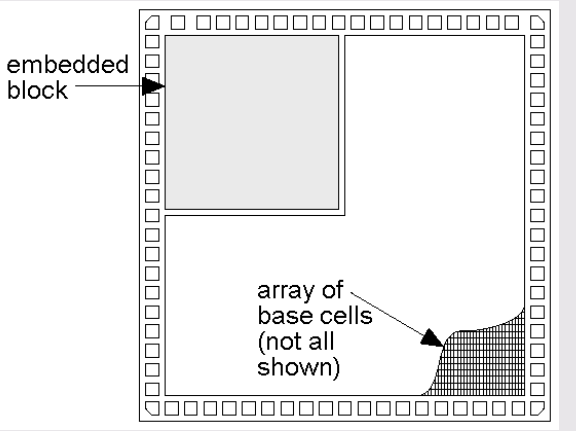

Figure 1.7 Gate array die with embedded block

Design Flow

1. **Design entry** - Using a hardware description language (HDL) or schematic entry
2. ***Logic synthesis*** - Produces a netlist - logic cells and their connections
3. ***System partitioning*** - Divide a large system into ASIC-sized pieces
4. **Prelayout simulation** - Check to see if the design functions correctly
5. ***Floorplanning*** - Arrange the blocks of the netlist on the chip
6. ***Placement*** - Decide the locations of cells in a block
7. ***Routing*** - Make the connections between cells and blocks
8. ***Extraction*** - Determine the resistance and capacitance of the interconnect
9. **Postlayout simulation** - Check to see the design still works with the added loads of the interconnect

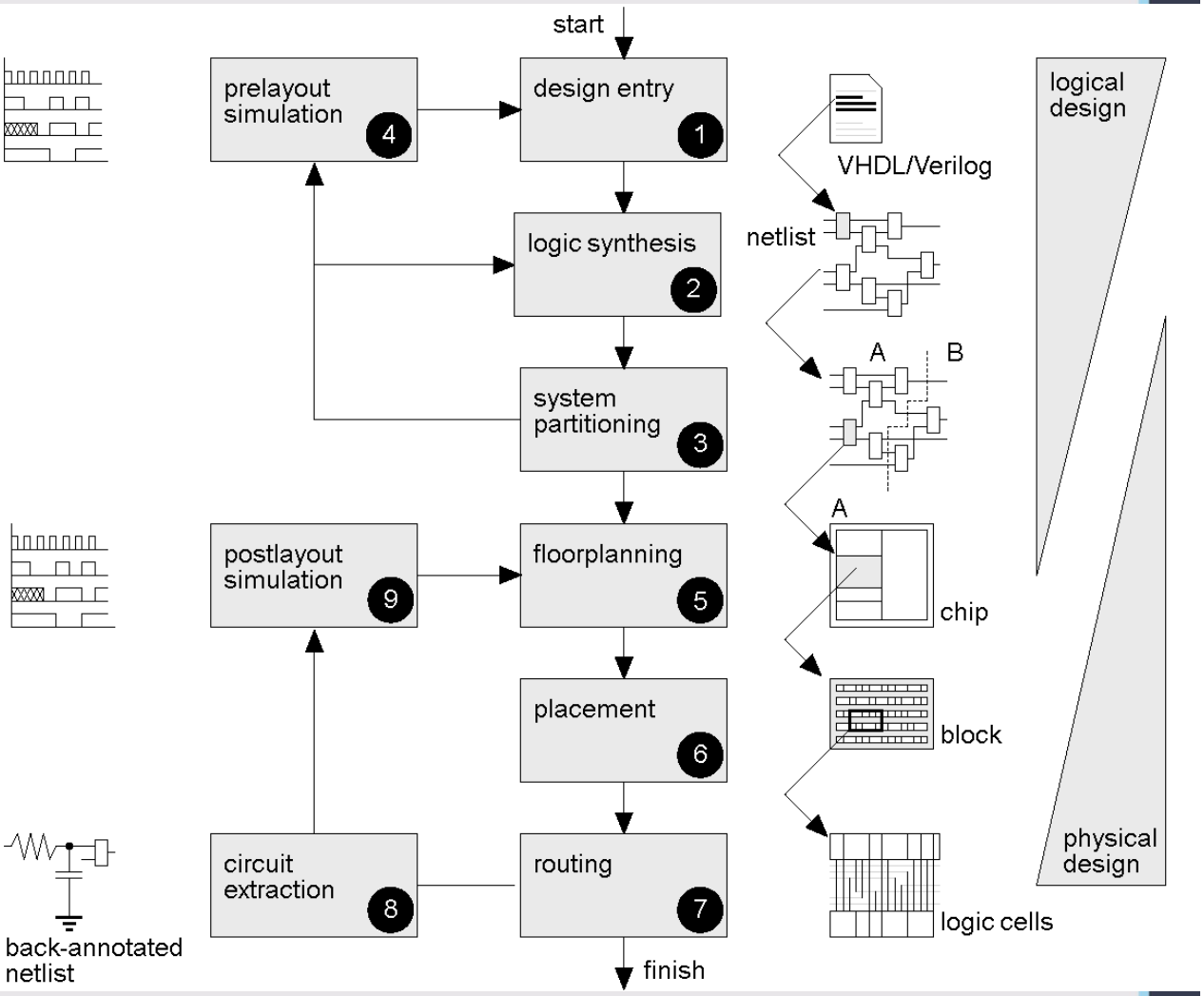

Figure 1.10 ASIC design flow

ASIC Fixed Costs

	FPGA		MGA		CBIC	
Training:	$800		$2,000		$2,000	
Days		2		5		5
Cost/day		$400		$400		$400
Hardware	$10,000		$10,000		$10,000	
Software	$1,000		$20,000		$40,000	
Design:	$8,000		$20,000		$20,000	
Size (gates)		10,000		10,000		10,000
Gates/day		500		200		200
Days		20		50		50
Cost/day		$400		$400		$400
Design for test:			$2,000		$2,000	
Days				5		5
Cost/day				$400		$400
NRE:			$30,000		$70,000	
Masks				$10,000		$50,000
Simulation				$10,000		$10,000
Test program				$10,000		$10,000
Second source:	$2,000		$2,000		$2,000	
Days		5		5		5
Cost/day		$400		$400		$400
Total fixed costs	$21,800		$86,000		$146,000	

Figure 1.12 Fixed costs analysis

ASIC Library Development

A complete ASIC library (suitable for commercial use) must include the following for each cell and macro:

- A physical layout
- A behavioral model
- A VHDL or Verilog model
- A detailed timing model
- A test strategy
- A circuit schematic
- A cell icon (symbol)
- A wire-load model
- A routing model